VERIFICATION OF TRANSLATION

I, Timothy S. Price, translator at Nakajima & Matsumura Patent Attorneys Office, 6F Yodogawa 5-Bankan, 3-2-1 Toyosaki, Kita-ku, Osaka, 531-0072, Japan, hereby declare that I am conversant with the English and Japanese languages and am a competent translator thereof. I further declare that to the best of my knowledge and belief the following is a true and correct translation made by me of a Japanese Patent Application No. 2003-340020 filed on September 30, 2003.

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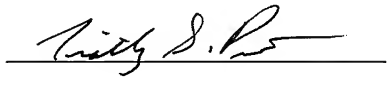

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[DOCUMENT] Claims

[CLAIM 1]

A semiconductor light emitting device comprising:

a substrate; and

a semiconductor multilayer film formed over a main surface of the substrate by crystal growth, the semiconductor multilayer film including a first conductive layer, a light emitting layer, and a second conductive layer in the stated order beginning on a substrate side, a portion of the semiconductor multilayer film from an outermost layer to at least the first conductive layer has been formed as a cylinder member having a substantially circular or *N*-sided polygonal cross-section, where *N* is an integer equal to or larger than five.

[CLAIM 2]

The semiconductor light emitting device of claim 1, further comprising:

a phosphor film that covers a main surface of the outermost layer of the semiconductor multilayer film, and a side surface of the cylinder member.

[CLAIM 3]

The semiconductor light emitting device of claim 2, wherein

a thickness of a portion of the phosphor film that covers the main surface of the outermost layer and a thickness of a portion of the phosphor film that covers the side surface of the cylinder member are substantially equal.

[CLAIM 4]

The semiconductor light emitting device of any of claims 1 to 3, wherein

the main surface of the substrate is rectangular in shape.

[CLAIM 5]

The semiconductor light emitting device of any of claims 1 to 4, wherein

a light reflective layer has been formed between the substrate and the first conductive layer.

[CLAIM 6]

The semiconductor light emitting device of any of claims 1 to 5, wherein

the cylinder member of the semiconductor multilayer film is divided into a plurality of areas by a division groove that reaches the substrate, the plurality of areas being a plurality of independent light emitting elements.

[CLAIM 7]

The semiconductor light emitting device of claim 6, wherein in each of the light emitting elements,

a first electrode has been formed on an exposed part of a main surface of the first conductive layer, the exposed part being created by partially removing the second conductive layer and the light emitting layer, and a second electrode has been formed on a

main surface of the second conductive layer, and

the plurality of light emitting elements are connected with each other in series in such a manner that a first electrode of one independent light emitting element is connected to a second electrode of another independent light emitting element using a wiring formed by a thin metal film.

[CLAIM 8]

The semiconductor light emitting device of claim 7, wherein

the light emitting layer included in each independent light emitting element has a substantially same area.

[CLAIM 9]

A light emitting module comprising:

a printed-wiring board; and

a semiconductor light emitting device as in any of claims 1 to 8, having been mounted on the printed-wiring board.

[CLAIM 10]

A lighting apparatus including, as a light source, a light emitting module as in claim 9.

[CLAIM 11]

A manufacturing method for a semiconductor light emitting device, comprising the steps of:

forming a multilayer semiconductor film over a main surface of a substrate by crystal growth, the semiconductor multilayer film

including a first conductive layer, a light emitting layer, and a second conductive layer in the stated order beginning on a substrate side;

dividing the semiconductor multilayer film into a plurality of cylinder members by removing a portion thereof from an outermost layer to at least the first conductive layer, each of the plurality of cylinder members having a substantially circular or *N*-sided polygonal cross-section, where *N* is an integer equal to or larger than five; and

dicing the substrate according to a plurality of areas including the cylinder members.

[CLAIM 12]

The manufacturing method for the semiconductor light emitting device of claim 11, further comprising the step of:

before the dicing step,

forming a phosphor film that covers a top face and a side face of each of the cylinder members.

[CLAIM 13]

The manufacturing method for the semiconductor light emitting device of claim 11 or 12, further comprising the step of:

dividing the semiconductor multilayer film into a plurality of areas including the cylinder members, by creating a groove in the semiconductor multilayer film that reaches the substrate.

[DOCUMENT] Specification

[TITLE OF THE INVENTION] Semiconductor light emitting device, light emitting module, lighting device, and manufacturing method for semiconductor light emitting device

[FIELD OF THE INVENTION]

[0001]

The present invention relates to a semiconductor light emitting device such as a light emitting diode (hereinafter, called an "LED") chip, a light emitting module and lighting device using the semiconductor light emitting device, and a manufacturing method for the semiconductor light emitting device.

[DESCRIPTION OF THE RELATED ART]

[0002]

In the field of LEDs, the brightness of white-light LEDs has been increasing in recent years, which has brought about active research into using such white-light LEDs for lighting purposes. LEDs are point light sources, and especially for such reason, focus has been placed on using LEDs for spot lighting in stores, art museums, showrooms, etc., as a substitute light source for halogen bulbs etc. which are conventionally widely used.

However, with conventional white-light LEDs, the spot shape of a beam shining on lit surface is rectangular, and this aspect must be addressed if LEDs are to be used for lighting purposes. The reason that the spot shape is rectangular is because the LED chip constituting a white-light LED is rectangular, and light is emitted

from a surface that is rectangular (e.g., see patent document 1). The shape of LED chips is as above due to manufacturing constraints.

[0003]

The following is an outline of a manufacturing method for LED chips. Firstly, a semiconductor multilayer film that includes a light emitting layer is formed on a substrate by crystal growth. A metallic electrode layer is formed thereon as necessary, whereafter mesa etching is used to form a lattice of grooves in the semiconductor multilayer film on the substrate. As a result, the semiconductor multilayer film is divided into diodes whose light emitting surface areas are the same several hundred microns square as a chip. After the characteristics of each diode have been tested, a diamond cutter is used to dice along the mesa-etched grooves that separate the diodes into chips, and then even deeper cuts are made. Lastly, the diodes are mechanically broken at the cut portions, thereby separating the diodes into individual chips. Thus the LED chips are completed.

[Patent document 1] Japanese Patent Application Publication No. 2001-15817

[DISCLOSURE OF THE INVENTION]

[PROBLEMS THE INVENTION IS GOING TO SOLVE]

[0004]

In order to obtain a circular spot shape for the beams emitted from LED chips, the chips need only be cut out into circular cylinder shapes from the substrate on which the semiconductor multilayer film has been formed. However, it is impossible to use a diamond cutter to make cuts that are circular with a diameter in the order of several

hundred microns. Also, although methods of polishing rectangularly cut LED chips into circular cylinder shapes are possible, such methods could hardly be said to be practical due to the size of the LED chips.

[0005]

In view of the above problem, an aim of the present invention is to provide a semiconductor light emitting device whose beam has a spot shape that is substantially circular or more like a circle than a rectangle, a manufacturing method for such semiconductor light emitting device, and a light emitting module and lighting device that use such semiconductor light emitting device.

[MEANS TO SOLVE THE PROBLEMS]

[0006]

In order to achieve the above aim, the present invention is a semiconductor light emitting device including: a substrate; and a semiconductor multilayer film formed over a main surface of the substrate by crystal growth, the semiconductor multilayer film including a first conductive layer, a light emitting layer, and a second conductive layer in the stated order beginning on a substrate side, a portion of the semiconductor multilayer film from an outermost layer to at least the first conductive layer has been formed as a cylinder member having a substantially circular or N-sided polygonal cross-section, where N is an integer equal to or larger than five.

[0007]

Also, the semiconductor light emitting device may further include a phosphor film that covers a main surface of the outermost layer of the semiconductor multilayer film, and a side surface of

the cylinder member.

Furthermore, a thickness of a portion of the phosphor film that covers the main surface of the outermost layer and a thickness of a portion of the phosphor film that covers the side surface of the cylinder member may be substantially equal.

Also, the main surface of the substrate may be rectangular in shape.

[0008]

Also, a light reflective layer may have been formed between the substrate and the first conductive layer.

Also, the cylinder member of the semiconductor multilayer film may be divided into a plurality of areas by a division groove that reaches the substrate, the plurality of areas being a plurality of independent light emitting elements.

Furthermore, in each of the light emitting elements, a first electrode may have been formed on an exposed part of a main surface of the first conductive layer, the exposed part being created by partially removing the second conductive layer and the light emitting layer, and a second electrode may have been formed on a main surface of the second conductive layer, and the plurality of light emitting elements may be connected with each other in series in such a manner that a first electrode of one independent light emitting element is connected to a second electrode of another independent light emitting element using a wiring formed by a thin metal film.

[0009]

Also, the light emitting layer included in each independent light emitting element may have a substantially same area.

In order to achieve the above aim, the present invention is also a light emitting module including: a printed-wiring board; and the above semiconductor light emitting device, having been mounted on the printed-wiring board.

In order to achieve the above aim, the present invention is also a lighting apparatus including, as a light source, the above light emitting module.

[0010]

In order to achieve the above aim, the present invention is also a manufacturing method for a semiconductor light emitting device, including the steps of: forming a multilayer semiconductor film over a main surface of a substrate by crystal growth, the semiconductor multilayer film including a first conductive layer, a light emitting layer, and a second conductive layer in the stated order beginning on a substrate side; dividing the semiconductor multilayer film into a plurality of cylinder members by removing a portion thereof from an outermost layer to at least the first conductive layer, each of the plurality of cylinder members having a substantially circular or N-sided polygonal cross-section, where N is an integer equal to or larger than five; and dicing the substrate according to a plurality of areas including the cylinder members.

[0011]

Also, the manufacturing method for the semiconductor light emitting device may further include the step of: before the dicing step, forming a phosphor film that covers a top face and a side face of each of the cylinder members.

Also, the manufacturing method for the semiconductor light

emitting device may further include the step of: dividing the semiconductor multilayer film into a plurality of areas including the cylinder members, by creating a groove in the semiconductor multilayer film that reaches the substrate.

[EFFECTS OF THE INVENTION]

[0012]

The semiconductor light emitting device of the present invention, the semiconductor multilayer film includes a first conductive layer, a light emitting layer, and a second conductive layer formed in the stated order beginning on the substrate side, and a portion of the semiconductor multilayer film from the outermost layer to at least the first conductive layer is formed as a cylinder member having a substantially circular or *N*-sided polygonal cross-section, where *N* is an integer equal to or larger than five. According to this construction, a spot shape of light emitted from the semiconductor light emitting device is like a circle or *N*-sided polygon, where *N* is an integer equal to or larger than five. Which is to say, the spot shape is more like a circle than a rectangle.

Also, since the light emitting module and lighting device of the present invention include the aforementioned semiconductor light emitting device, a spot shape of light emitted therefrom is more like a circle than a rectangle.

Also, the manufacturing method for a semiconductor light emitting device of the present invention includes the steps of: forming a multilayer semiconductor film over a main surface of a substrate by crystal growth, the semiconductor multilayer film

including a first conductive layer, a light emitting layer, and a second conductive layer in the stated order beginning on a substrate side; and dividing the semiconductor multilayer film into a plurality of cylinder members by removing a portion thereof from an outermost layer to at least the first conductive layer, each of the plurality of cylinder members having a substantially circular or N-sided polygonal cross-section, where N is an integer equal to or larger than five. This achieves a manufacturing method for a semiconductor light emitting device that has the aforementioned effects.

[EMBODIMENTS OF THE INVENTION]

[0013]

The following describes an embodiment of the present invention with reference to the drawings.

Fig.1 is an external perspective view illustrating a construction of an LED array chip 2 which is one type of a semiconductor light emitting device. Fig.2 is a plan view illustrating the LED array chip 2. Fig.1 mainly intends to illustrate how LEDs D1 to D36 (described later) are arranged, and therefore does not show minute depressions and protrusions on the surfaces of the LEDs. Fig.2 does not show a phosphor film 50 (shown in Fig.1 and mentioned later) and depressions formed on a p-electrode (mentioned later).

[0014]

As shown in Figs.1 and 2, the LED array chip 2 is formed in such a manner that a semiconductor multilayer film including a light emitting layer is formed on a non-doped (high-resistive) SiC substrate 4 which is a semiconductor substrate (hereinafter referred

to as "an SiC substrate 4"). Here, the semiconductor multilayer film is formed like a circular cylinder as a whole. The circular-cylinder-like semiconductor multilayer film formed on the rectangular (square in the present embodiment) SiC substrate 4 is hereinafter referred to as a cylinder member 6. The cylinder member 6 is divided into a plurality of areas (12 areas in the present embodiment) by division grooves 8 that radiate equiangularly. Which is to say, the cylinder member 6 is divided into 12 flabellate members with a central angle of around 30 degrees. Each flabellate member is further divided into a plurality of areas (three areas in the present embodiment) in a diameter direction by two division grooves 10 and 11 that are formed concentrically. As a result, the cylinder member 6 formed by the semiconductor multilayer film is divided into 36 areas (12×3), and each area constitutes an independent light emitting element, i.e. an LED. The 36 LEDs are respectively identified by reference marks D1 to D36 as shown in Fig.1 to be distinguished from each other.

[0015]

The concentrical division grooves 10 and 11 are respectively positioned so that a light emitting layer of each of the LEDs D1 to D36 has the substantially same area. This is achieved when the ratio of L1:L2:L3 (lengths L1, L2 and L3 are shown in Fig.2) is $1:\sqrt{2}:\sqrt{3}$, irrespective of a size (a diameter) of the cylinder member 6. The SiC substrate 4 is a square approximately 2 mm on a side, and the cylinder member 6 has a diameter of approximately 1.8 mm.

[0016]

The following part describes a construction of each LED

in the LED array chip 2 with reference to cross-sectional views in Fig.3.

Fig.3A illustrates a cross-section of LEDs D1 and D2 in the LED array chip 2 along a line A-A shown in Fig.2, and Fig.3B illustrates a cross-section of LEDs D35 and D36 along a line B-B shown in Fig.2. Each of the LEDs D1 to D36 is formed by a semiconductor multilayer film having the same construction. The following description is made taking the LED D35 as an example.

[0017]

Each LED is made up of an n-AlGaN buffer layer 12 (having a thickness of 30 nm), a DBR (Distributed Bragg Reflector) layer 14 composed of 30 periods of n-AlGaN/GaN (having a total thickness of 3 μm), an n-GaN clad layer 16 (having an Si-doping amount of 3×10^{18} cm^{-3} and a thickness of 200 nm), an InGaN/GaN MQW (Multiple Quantum Well) light emitting layer 18 composed of six periods of InGaN (having a thickness of 2 nm)/GaN (having a thickness of 8 nm), a p-GaN clad layer 20 (having an Mg-doping amount of 1×10^{19} cm^{-3} and a thickness of 200 nm), a p-GaN contact layer 22 (having an Mg-doping amount of 3×10^{19} cm^{-3} and a thickness of 200 nm), and an n^+-GaN regrowth layer 24 (having an Si-doping amount of 1×10^{19} cm^{-3} and a thickness of 100 nm). These layers 12, 14, 16, 18, 20, 22 and 24 are formed on the SiC substrate 4 in the stated order. Which is to say, a light emitting layer (the MQW light emitting layer 18) is sandwiched between a conductive layer (the n-GaN clad layer 16 on a side of the SiC substrate 4) and a conductive layer (the p-GaN clad layer 20, the p-GaN contact layer 22 and the n^+-GaN regrowth layer 24 on a side of a light extraction surface) in each of the LEDs D1 to D36.

A Ti/Au p-electrode 26 is formed on the n^+-GaN regrowth layer 24 and the p-GaN contact layer 22. A Ti/Au n-electrode 28 is formed on the n-GaN clad layer 16.

[0018]

When power is supplied to this LED through the p-electrode 26 and the n-electrode 28, the light emitting layer 18 emits blue light having a wavelength of 460 nm.

Depressions are formed at a predetermined interval on an upper surface of the p-electrode 26, which is a light extraction surface, in order to improve light extraction efficiency. The depressions are provided by forming the n^+-GaN regrowth layer 24 partially on the p-GaN contact layer 22 in a manner described later.

[0019]

It should be noted that each of the semiconductor layers 12, 14, 16, 18, 20, 22 and 24 making up the semiconductor multilayer film that emits blue light may have a different composition. Each layer may be made of a III-V nitride semiconductor which is generally represented by a chemical formula of $B_zAl_xGa_{1-x-y-z}In_yN_{1-v-w}As_vP_w$, where $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$, $0 \leq x+y+z \leq 1$, $0 \leq v \leq 1$, $0 \leq w \leq 1$, $0 \leq v+w \leq 1$ (generally represented as BAlGaInNAsP and hereinafter referred to as a GaN semiconductor material). It is known that the GaN semiconductor material can emit light having a wavelength within a wide range of 200 nm (ultraviolet light) and 1700 nm (infrared light) depending on its composition. In recent years, the GaN semiconductor material has been commonly used to produce light having a shorter wavelength than blue-green light.

[0020]

The 36 LEDs D1 to D36 described above are connected in series on the SiC substrate 4. The following part describes how the LEDs D1 to D36 are connected to each other.

As shown in Figs.3A and 3B, an Si_3N_4 insulating film 30 is formed so as to cover side surfaces of the LEDs D1, D2, D35 and D36 and the division groove 11. On the insulating film 30, a wiring 32a, which is formed by a Ti/Pt/Au metal thin film, is provided to connect an n-electrode 28a of the LED D1 and a p-electrode 26B of the LED D2. Likewise, a wiring 32b is formed on the insulating film 30 to connect an n-electrode 28c of the LED D35 and a p-electrode 26d of the LED D36. In the same manner, the LEDs D2 to D35 are connected by a wiring 22. As shown in Fig.2, for example, an n-electrode 28e of the LED D3 and a p-electrode 26f of the LED D4 are connected by a wiring 32C. An n-electrode 28g of the LED D6 and a p-electrode 26h of the LED D7 are connected by a wiring 32d. Thus, all of the LEDs D1 to D36 are connected in series as shown in Fig.4A.

Out of the 36 LEDs that are connected in series in the LED array chip 2, the LED D1 is an LED on a higher potential end. Therefore, a p-electrode 26a of the LED D1 is an anode electrode of the LED array chip 2. The LED D36 is an LED on a lower potential end. Therefore, an n-electrode 28d of the LED D36 is a cathode electrode of the LED array chip 2.

[0021]

As shown in Fig.2, Ti/Pt/Au conductive patterns 34 and 36 are formed, so as to surround the semiconductor multilayer film, on a front main surface, of the SiC substrate 4, on which the semiconductor multilayer film is formed. The conductive pattern 34

is connected to the p-electrode of the LED D1 by a wiring 32e, and the conductive pattern 36 is connected to the n-electrode 28d of the LED D36 by a wiring 32f.

[0022]

Fig.4B illustrates a back main surface of the LED array chip 2. As shown in Fig.4B, two Ti/Pt/Au power supply terminals 38 and 40 are formed on a main surface of the SiC substrate 4 which is opposite to the front main surface on which the LEDs D1 to D36 are formed.

The power supply terminal 38 is connected to the conductive pattern 34 by two through holes 42 and 44 provided in the SiC substrate 4. Similarly, the power supply terminal 40 is connected to the conductive pattern 36 by two through holes 46 and 48 provided in the SiC substrate 4. Thus, the power supply terminal 38 is electrically connected to the p-electrode 26a of the LED D1, and the power supply terminal 40 is electrically connected to the n-electrode 28d of the LED D36. The through holes 42, 44, 46 and 48 are each formed by filling a hole having a diameter of 30 μm provided in the SiC substrate 4 with Pt. When an electric current of 50 mA is applied to the 36 LEDs that are connected in series through the power supply terminals 38 and 40 with heat dissipation being ensured, an operation voltage of 120 V is observed.

[0023]

Furthermore, each of the LEDs D1 to D36 can produce an even amount of light. This is because the light emitting layer 18 in each of the LEDs D1 to D36 has substantially the same area, and an electric density of each LED is therefore substantially the same. As a result,

unevenness of illuminance on a surface to which light from the LED array chip 2 is irradiated can be prevented.

The phosphor film 50 is formed on the front main surface of the SiC substrate 4 so as to cover an upper surface and a side surface of the cylinder member 6 (the semiconductor multilayer film). The phosphor film 50 is made of a light-transmitting resin such as silicone in which particles of a yellow phosphor $(Sr, Ba)_2SiO_4:Eu^{2+}$ and fine particles of SiO_2 are dispersed. The phosphor film 50 is applied at a substantially even thickness of approximately 50 μm on and around the cylinder member 6. Here, the light-transmitting resin may be an epoxy resin or a polyimide resin instead of silicone.

[0024]

The light emitting layer 18 of each of the LEDs D1 to D36 emits blue light, and the phosphor within the phosphor film 50 converts part of the blue light into yellow light. The blue light and the yellow light mix together, to generate white light.

In the LED array chip 2, the semiconductor multilayer film including a light emitting layer is formed like a circular cylinder, and the phosphor film 50 is applied on and around the semiconductor multilayer film, at a substantially even thickness. Which is to say, the phosphor film 50 is formed like a circular-cylindrical case with bottoms. Thus, a spot shape of light emitted from the LED array chip 2 is substantially circular. With this feature, the LED array chip 2 is suitable as a light source for lighting. In addition, the DBR layer 14, which is a light-reflective layer, is formed between the light emitting layer 18 and the SiC substrate 4. The DBR layer 14 reflects, towards a light extraction surface, 99% or more of blue

light emitted from the light emitting layer 18 towards the SiC substrate 4. This improves light extraction efficiency of each LED in the LED array chip 2. The phosphor film 50 covers, at the same thickness, not only the upper surfaces of the outmost LEDs D1, D6, D7, D12, D15, D18, D19, D24, D25, D30, D31 and D36 but also outer side surfaces of these outmost LEDs. Accordingly, the phosphor film 50 converts, into yellow light, not only blue light emitted from the upper surface of each of these LEDs but also blue light emitted from the side surface of the light emitting layer 18 of each of these LEDs. Thus, unevenness of color can be reduced. In this description, blue light indicates light having a wavelength from 400 nm inclusive to 500 nm exclusive, and yellow light indicates light having a wavelength from 550 nm inclusive to 600 nm exclusive. According to the above description, the LEDs D1 to D36 each emit light with a peak emission wavelength of 460 nm. However, the LEDs D1 to D36 may be configured to emit light with a different peak emission wavelength within the above-mentioned range.

[0025]

It is generally accepted that unevenness of color occurs only in a white LED that uses visible light having a spectral component of a wavelength within a range of 380 nm and 780 nm (purple to red) for an excitation light source. In other words, unevenness of color does not occur in a white LED having near-ultraviolet light as an excitation light source. However, ultraviolet light with a peak emission wavelength of 370 nm also has a spectral component of a wavelength no less than 380 nm (visible light). Therefore, a white LED using near-ultraviolet light as an excitation light source can

in reality have a problem of unevenness of color, depending on a ratio of spectral components of a wavelength no less than 380 nm. Accordingly, the present embodiment is applicable to an LED having a light emitting layer that emits near-ultraviolet light to achieve the same effects of reducing unevenness of color for the same reasons stated above. Which is to say, the present embodiment of the present invention is applicable to an LED including a light emitting layer that emits light including a spectral component of a wavelength at least within a range of 380 nm and 780 nm to reduce unevenness of color. The application of the present embodiment is not limited to an LED including a light emitting layer that emits blue light having a peak emission wavelength of 460 nm as describe above.

[0026]

The following part describes a manufacturing method for the LED array chip 2 described above.

The manufacturing method of the LED array chip 2 includes a variety of processes. The following part first describes a process of forming the cylinder member 6 (shown in Fig.1), with reference to Figs.5 to 9.

To start with, a semiconductor multilayer film is formed on an upper main surface of a non-doped SiC substrate 104 shown in Fig.5A (hereinafter simply referred to as "a substrate 104").

[0027]

After this, an etching resist (a positive resist) is applied on the entire upper main surface, of the substrate 104, on which the semiconductor multilayer film is formed, and the etching resist is then heated to be cured. Thus, a resist film 61 is formed as shown

in Fig.5B.

After this, a photomask 59 is placed on the substrate 104 as shown in Fig.6. The photomask 59 is formed by printing a pattern 591 in black on a glass plate. The pattern 591 is formed in such a manner that a plurality of patterns 592 shown in Fig.7A are closely arranged in a matrix. The resist film 61 is exposed using a mercury lamp while the photomask 59 is placed on the substrate 104. Thus, areas of the resist film 61 which correspond to not-printed transparent portions (white portions shown in Fig.7A) of the photomask 59 are softened. The softened areas of the resist film 61 are dissolved by an organic solvent, to be removed. Thus, a resist mask 63 shown in Fig.8A is formed.

[0028]

After the resist mask 63 is formed, an Au film is formed on the entire upper main surface of the substrate 104 by deposition. Subsequently, a portion of the Au film which is formed on the resist mask 63 is removed together with the resist mask 63 by an organic solvent that can dissolve the cured resist mask 63. Thus, as shown in Fig.8B, metal masks 58 are formed at locations of white circles shown in Fig.8A. Each metal mask 58 masks an area in which the cylinder member 6 is to be formed. In more detail, each metal mask 58 masks the white portions shown in Fig.7A. An unmasked area of the semiconductor multilayer film formed on the substrate 104 is removed by dry etching to such a depth that the n-GaN clad layer 16 (shown in Fig.3B) is exposed. The dry etching is conducted by leaving the substrate 104 within a gas including chlorine ions for a predetermined time. Thus, cylinder members each having a substantially half height

of the cylinder member 6 (hereinafter referred to as half cylinder members 600 shown in Figs.9A and 9B) are formed. After the dry etching is completed, the metal masks 58 are removed by an iodine solvent.

[0029]

By the above-described etching step (hereinafter referred to as "a first etching step"), the half cylinder members 600 are formed as shown in Figs.9A and 9B. Fig.9A illustrates part of a cross-section along a line G-G shown in Fig.9B, and Fig.9C is an enlargement view illustrating a portion H shown in Fig.9B.

After the first etching step, a second etching step is conducted to remove portions of the semiconductor multilayer film which do not constitute the half cylinder members 600. Thus, cylinder members 6 (shown in Fig.1) are formed on the substrate 104. The reason for conducting the first and second etching steps to form the cylinder members 6 is explained later. The second etching step is the same as the first etching step except for that the photomask 59 (shown in Fig.6) has a different pattern. Accordingly, the second etching step is not repeatedly described in detail here, and only briefly mentioned in the following description of the manufacturing method of the LED array chip 2. The following description is made with a particular focus on each one of the LED array chips 2 on the substrate 104.

[0030]

The following part describes how each one of the LED array chips 2 is manufactured, with reference to Figs.10 to 13.

In Figs.10 to 13, a material to form each constituent of the LED array chip 2 is identified by a three-digit number whose

first digit is one. The last two digits of the three-digit number represents a reference numeral identifying the corresponding constituent of the LED array chip 2. Figs.10 to 13 each illustrate a cross-section along a line C-C shown in Fig.2.

[0031]

Firstly, as shown in Fig.10, an n-AlGaN buffer layer 112, a DBR layer 114 composed of 30 periods of n-AlGaN/GaN, an n-GaN clad layer 116, an InGaN/GaN MQW light emitting layer 118, a p-GaN clad layer 116, and a p-GaN contact layer 122 are formed on the non-doped SiC substrate 104 in the stated order using a MOCVD (Metal Organic Chemical Vapor Deposition) method (step A). Here, the non-doped SiC substrate 104 has a diameter of two inches and a thickness of 300 μm.

[0032]

After this, an SiO_2 film 54 is formed on the p-GaN contact layer 122, and a photoresist layer is then formed on the SiO_2 film 54 in the following manner. A parallel-line pattern in which lines are arranged at a predetermined interval (e.g. 1200 lines/mm) is formed by interferometric exposure using a He-Cd laser beam. This is conducted three times, and any two of the three parallel-line patterns intersect with each other at an angle of 120 degrees. Thus, a resist mask 56 is formed (step B).

[0033]

A portion of the SiO_2 film 54 which is not masked by the resist mask 56 is removed by etching (step C). Then, the resist mask 56 is removed (step D).

After this, an n^+-GaN layer 124 is regrown using a MOCVD

method (step E). Here, a portion of the n^+-GaN layer 124 formed on the SiO_2 film 54 is not shown in the step E shown in Fig.11.

[0034]

The portion of the n^+-GaN layer 124 formed on the SiO_2 film 54 is then removed together with the SiO_2 film 54 (step F).

The next step G is the first etching step described above. The step G is conducted to create a surface to connect the n-electrode 28 (shown in Fig.3). Firstly, the Au metal mask 58 is formed in the above-described manner.

[0035]

The metal mask 58 masks an area in which the p-electrode 26 of each LED is to be formed. An unmasked area of a lamination composed of the layers 112 to 124 is removed by dry etching to a depth of an approximately half of the thickness of the n-GaN clad layer 116 (step G). Thus, a surface 60 to connect the n-electrode 28 is created. The metal mask 58 is removed prior to the next step H.

The step H is the second etching step mentioned above, and conducted to create a surface to form the conductive patterns 34 and 36, and the division grooves 8, 10 and 11. To be specific, a metal mask 62 is formed so as to mask the resulting surface after the step G except for areas in which the conductive patterns 34 and 36 and the division grooves 8, 10 and 11 are to be formed. As mentioned above, this metal mask 62 formation step (step H) is the same as the first etching step (the step G) except for that the photomask 59 (shown in Fig.6) which is used for exposure of the resist film 61 has a different pattern. Fig.7B illustrates a pattern used in

the metal mask 62 formation step. Regarding Fig.7B, 12 radiating bold lines 108 correspond to areas in which the division grooves 8 (see Fig.2) are to be formed. Two bold concentrical circles 110 and 111 respectively correspond to areas in which the division grooves 10 and 11 (see Fig.2) are to be formed. A black area surrounding a white area formed like a circle corresponds to an area in which a surface to form the conductive patterns 34 and 36 is to be created. Which is to say, the metal mask 62 is formed so as to mask areas which correspond to constituents of the cylinder member 6.

Unmasked areas of a lamination composed of the rest of the layer 116 and the layers 114 and 112 are removed by dry etching to such a depth that the substrate 104 is exposed, to create the conductive pattern formation surface 64 and the division groove 11 (8 and 10). At the same time, the cylinder member 6 (see Fig.1) is formed (step H). After the dry etching, the metal mask 62 is removed prior to the next step. As seen from the above description of the steps G and H, the cylinder member 6 is formed by conducting two different etching steps to create the surface to form the n-electrode 28, which is positioned on the n-GaN clad layer 16.

[0036]

Subsequent to the step H, an Si_3N_4 insulating film 130 is formed by sputtering or the like for insulation and surface protection (step I).

A mask 66 is then formed so as to mask the Si_3N_4 film 130 except for an area in which the p-electrode 26 is to be formed. An unmasked area of the Si_3N_4 film 130 is removed by etching. After this, a Ti/Au thin film 126 is applied by deposition. Thus, the Ti/Au

p-electrode 26 is formed (step J). A portion of the Ti/Au thin film 126 formed on the mask 66 (not shown in Fig.12) is removed together with the mask 66 prior to the next step. Here, the p-electrode 26 may be formed by an ITO transparent thin film, instead of the Ti/Au thin film.

[0037]

The same procedure as in the step J is conducted to form the n-electrode 28. Specifically speaking, a mask 68 is formed so as to mask the resulting surface after the step J, except for an area in which the n-electrode 28 is to be formed. An unmasked area of the Si_3N_4 film 130 is removed by etching, and then a Ti/Au thin metal film 128 is formed by deposition. Thus, the n-electrode 28 is formed (step K). A portion of the Ti/Au film 128 formed on the mask 68 (not shown in Fig.12) is removed together with the mask 68 prior to the next step.

[0038]

After this, a mask 70 is formed so as to mask the resulting surface after the step K except for an area in which each of the through holes 42, 44, 46 and 48 is to be formed. An unmasked area is removed by etching, to form an opening 72 that is 200 μm in depth. Then, the opening 72 is filled with Pt by electroless deposition or the like (step L). The mask 70 is removed prior to the next step.

Subsequently, a mask 74 is formed so as to mask the resulting surface after the step L, except for areas in which the conductive patterns 34 and 36 and the wiring 32 are to be formed. Then, a Ti/Pt/Au thin metal film is formed by deposition. Thus, the Ti/Pt/Au conductive patterns 34 and 36 and the Ti/Pt/Au wiring 32 are formed (step M).

A portion of the Ti/Pt/Au film which is formed on the mask 74 (not shown in Fig.13) is removed together with the mask 74 prior to the next step.

After this, a lower main surface of the SiC substrate 104 is polished, so that the thickness of the SiC substrate 104 becomes 150 μm and the through holes 42, 44, 46 and 48 are exposed on the lower main surface of the SiC substrate 104 (step N).

Subsequently, a mask 76 is formed so as to mask the lower main surface of the SiC substrate 104 except for areas in which the power supply terminals 38 and 40 are to be formed. Then, a Ti/Pt/Au thin metal film is formed on the lower main surface of the SiC substrate 104 by deposition. Thus, the Ti/Pt/Au power supply terminals 38 and 40 are formed (step O). A portion of the Ti/Pt/Au film which is formed on the mask 76 (not shown in Fig.13) is removed together with the mask 76 prior to the next step.

After this, the phosphor film 50 is formed in the following manner. A silicone resin in which particles of a yellow phosphor $(Sr, Ba)_2SiO_4:Eu^{+2}$ and fine particles of SiO_2 are dispersed is applied by printing, and then heated to be cured. After being cured, the phosphor film 50 is polished so that a thickness of the phosphor film 50 in a direction perpendicular to the upper main surface of the SiC substrate 104 becomes 50 μm (step P). Here, a color temperature of white light emitted from the LED array chip 2 is determined by a ratio between a quantity of blue light from the light emitting layer 18 and that of yellow light from the phosphor film 50. The ratio is adjusted by a percentage of the phosphor particles in the silicone resin and the thickness of the phosphor film 50. To be specific,

when the percentage of the phosphor particles is higher or the thickness of the phosphor film 50 is larger, the ratio of the yellow light is higher. Here, a high ratio of the yellow light means that the white light has a lower color temperature. As described above, the phosphor film 50 is formed in such a manner that the silicone resin including the phosphor is first applied at a thickness larger than a designed thickness, and then polished to have the designed thickness. This enables the phosphor film 50 to be formed at an even thickness and to have the designed thickness. As a result, unevenness of color can be reduced, and a desired color temperature can be exactly achieved.

Lastly, the substrate 104 is divided into individual LED array chips 2 by dicing. In this way, the LED array chip 2 (shown in Fig.1) is manufactured.

[0039]

Fig.14 is an external perspective view illustrating a white LED module 200 including LED array chips 2 described above (hereinafter simply referred to as "an LED module 200"). The LED module 200 is attached to a lighting unit 240 (mentioned later).

The LED module 200 includes a ceramics substrate 202 that is in a shape of a circle having a diameter of 5 cm and is made of AlN and three lenses 204, 206 and 208 made of glass. A guiding depression 210 used to attach the LED module 200 to the lighting unit 240 and terminals 212 and 214 to receive a power supply from the lighting unit 240 are provided in the ceramics substrate 202.

[0040]

Fig.15A is a plan view illustrating the LED module 200,

Fig.15B illustrates a cross-section of the LED module 200 along a line E-E shown in Fig.15A, and Fig.15C is an enlargement view illustrating a portion F shown in Fig.15B.

As shown in Figs.15A and 15B, a guiding hole (a through hole) 216 is provided in the center of the ceramics substrate 202 to attach the LED module 200 to the lighting unit 240. As shown in Fig.15C, a gold plating 217 is applied to a lower surface of the ceramics substrate 202 for improving heat dissipation.

[0041]

The LED array chip 2 is mounted at a location, on an upper surface of the ceramics substrate 202, corresponding to a center of each of the lenses 204, 206 and 208 having a shape of a circle as shown in Fig.15A. In total, three LED array chips 2 are mounted on the ceramics substrate 202.

The ceramics substrate 202 is made up of two ceramics substrates 201 and 203 each of which has a thickness of 0.5 mm and is mainly made of AlN. The ceramics substrates 201 and 203 may be made of Al_2O_3, BN, MgO, ZnO, SiC and diamond, instead of AlN.

[0042]

The LED array chips 2 are mounted on the lower ceramics substrate 201. Taper through holes 215 are provided in the upper ceramics substrate 203, so as to create spaces for mounting the LED array chips 2.

A cathode pad 218 and an anode pad 220 (shown in Fig.16B) are provided at the location, on an upper surface of the ceramics substrate 201, where each LED array chip 2 is to be mounted. Each of the cathode pad 218 and the anode pad 220 is made up of nickel

(Ni) plating and then gold (Au) plating applied on copper (Cu). The LED array chip 2 is mounted on the ceramics substrate 201 in such a manner that the SiC substrate 4 is adhered to the ceramics substrate 201. Here, the power supply terminals 36 and 38 are respectively connected to the cathode pad 218 and the anode pad 220 using solder. Instead of solder, a gold bump or a silver paste may be used.

[0043]

In the LED array chip 2, no components that block light, such as a bonding wire, exist on or above a light extraction surface. Therefore, light emitted from the LED array chip 2 does not contain shadow. This feature is highly valuable for a light source used for lighting.

Before being mounted, the LED array chips 2 have been tested for their optical performance, such as unevenness of color, and have passed the test. According to the present embodiment, the LED array chip 2 includes the phosphor film 50, and can emit white light by itself. As describe above, this makes it possible to test the LED array chip 2 for its optical performance before the LED array chip 2 is mounted. Consequently, it can be prevented that the LED module 200 including the LED array chips 2 is rejected due to poor optical performance of the LED array chips 2. As a result, the ratio of accepted finished products (LED modules 200) to all finished products can be improved.

[0044]

An aluminum reflection film 219 is formed on a wall of each through hole 215 provided in the upper ceramics substrate 203 and on an upper surface of the ceramics substrate 203.

The lenses 204, 206 and 208 are adhered to the ceramics substrate 203 using an adhesive agent 221. The adhesive agent 221 may be a silicone resin, an epoxy resin or the like.

[0045]

The three LED array chips 2 are connected in parallel by a wiring pattern formed on the upper surface of the ceramics substrate 201.

Fig.16A is a plan view illustrating the LED module 200 after removing the lenses 204, 206 and 208. In Fig.16A, the three LED array chips 2 are distinguished from each other by addition of marks of A, B and C.

[0046]

As described above, the anode pad 220 and the cathode pad 218 (Fig.16B) are provided at the location, on the upper surface of the ceramics substrate 201, where each of the LED array chips 2A, 2B and 2C is mounted.

The anode pads 220 that are respectively connected to the LED array chips 2A, 2B and 2C are electrically connected to each other by a wiring pattern 236. The wiring pattern 236 is connected to the positive terminal 212 at its end by a through hole 237. The cathode pads 218 that are respectively connected to the LED array chips 2A, 2B and 2C are electrically connected to each other by a wiring pattern 238. The wiring pattern 238 is connected to the negative terminal 214 at its end by a through hole 239. In other words, the LED array chips 2A, 2B and 2C are connected in parallel by the wiring patterns 236 and 238.

[0047]

The LED module 200 described above is attached to the lighting unit 240. The LED module 200 and the lighting unit 240 constitute a lighting apparatus 242.

Fig.17A is a schematic perspective view illustrating the lighting apparatus 242, and Fig.17B is a bottom plan view illustrating the lighting apparatus 242.

[0048]

The lighting unit 240 is, for example, fixed on a ceiling of a room. The lighting unit 240 includes a power supply circuit (not shown in Figs.17A and 17B) that converts alternating-current power (e.g. 100 V, 50/60Hz) supplied from a commercial power source into direct-current power required for driving the LED module 200.

The following part describes a construction to attach the LED module 200 to the lighting unit 240, with reference to Fig.18.

[0049]

The lighting unit 240 has a circular depression 244 in which the LED module 200 is to be fitted. A bottom surface of the circular depression 244 is flat. An internal thread (not shown in Fig.18) is created, in the vicinity of an open end of the circular depression 244, on an inside wall of the circular depression 244. Flexible power supply terminals 246 and 248 and a guiding protrusion 230 protrude from the inside wall of the circular depression 244, between the internal thread and the bottom surface of the circular depression 244. The power supply terminals 246 and 248 are respectively positive and negative. A guiding pin 252 is provided in the center of the bottom surface of the circular depression 244.

[0050]

An O-ring 254 made of silicon rubber and a ring screw 256 are used to attach the LED module 200 to the lighting unit 240. The ring screw 256 has a shape of a ring that has a substantially rectangular cross-section. An external thread (not shown in Fig.18) is created on an outer surface of the ring screw 256, and a depression 258 is provided.

[0051]

The following part describes a procedure of attaching the LED module 200 to the lighting unit 240.

To start with, the LED module 200 is fitted in the circular depression 244 in the following manner. The ceramics substrate 202 of the LED module 200 is positioned between the bottom surface of the circular depression 244 and the power supply terminals 246 and 248. The guiding pin 252 is fitted in the guiding hole 216, so as to align the center of the LED module 200 with the center of the circular depression 244. Furthermore, the guiding protrusion 230 is fitted in the guiding depression 210, so as to align the positive and negative terminals 212 and 214 with the power supply terminals 246 and 248 respectively.

[0052]

After the LED module 200 is fitted in the circular depression 244, the ring screw 256 to which the O-ring 254 has been attached is screwed into the circular depression 244 and fixed. Thus, the positive and negative terminals 212 and 214 are respectively connected to the power supply terminals 246 and 248, so that the terminals 212 and 214 are electrically connected to the terminals 246 and 248 reliably. In addition, the substantially entire lower

surface of the ceramics substrate 202 is connected to the flat bottom surface of the circular depression 244. This enables heat generated in the LED module 200 to be effectively conducted to the lighting unit 240, thereby improving a cooling effect of the LED module 200. Here, silicone grease may be applied to the lower surface of the ceramics substrate 202 and the bottom surface of the circular depression 244 to further improve the heat conduction efficiency from the LED module 200 to the lighting unit 240.

[0053]

When power is supplied to this lighting apparatus 242 from a commercial power source, each blue LED 6 in the LED array chip 2 emits blue light. Here, part of the blue light is converted into yellow light by the phosphor within the phosphor film 50. The blue light and the yellow light mix together, to generate white light. The white light is emitted through the lenses 204, 206 and 208.

[0054]

As described above, a spot shape of the white light generated by the LED array chip 2 is substantially circular. The lighting apparatus 242 including a plurality of LED array chips 2 (three chips 2 in the present embodiment) can also produce light which has a substantially circular spot shape when irradiated to a surface positioned distant enough from the lighting apparatus 242 in relation to a diameter of each of the lenses 204, 206 and 208 and an interval between any two of the lenses 204, 206 and 208.

When an electric current of 150 mA is applied to the LED module 200, a total luminous flux of 800 lm, an on-axis luminous intensity of 1500 cd, and an emission spectrum shown in Fig.19 are

observed.

[0055]

It should be noted that the present invention is not limited to the above-described embodiment. The present invention includes the following modification examples.

(1) According to the embodiment, the semiconductor multilayer film is formed like a circular cylinder. However, the embodiment is not limited to such. The semiconductor multilayer film may be formed like a cylinder with *N*-sided polygons for bases, where *N* is an integer equal to or larger than five. In this way, a spot shape of light emitted from the LED array chip is more like a circle than a rectangle. In addition, it is preferable that the semiconductor multilayer film is formed as a cylinder with regular *N*-sided polygons for bases, where *N* is an even integer. In this way, the spot shape of light emitted from the LED array chip can be point-symmetric, such as a circle.

(2) According to the embodiment, light emitted from the light emitting module or the lighting apparatus has a circular (point-symmetric) spot shape, as a circular spot shape of light emitted from each LED array chip (semiconductor light emitting device) is scarcely worsened. However, the light emitted from the light emitting module or the lighting apparatus may be required to have a point-asymmetric spot shape, depending on use of the light emitting module or the lighting apparatus. The semiconductor light emitting device can easily produce light having a desired point-asymmetric spot shape since it is comparatively easy to convert light with a point-symmetric spot shape into light with a desired

point-asymmetric spot shape. This conversion is achieved by providing a known mechanism for converting a point-symmetric spot shape into a desired spot shape, on the light extraction side of the semiconductor light emitting device. When such a mechanism is provided, the lighting apparatus is, for example, used for a head lamp of a car.

(3) According to the embodiment, the circular-cylinder-like semiconductor multilayer film is divided into 36 portions, to form 36 independent LEDs (light emitting elements). However, the number of the independent LEDs is not limited to 36.

Alternatively, the cylinder-like semiconductor multilayer film may not be divided. Which is to say, an LED chip that is constituted by one LED (light emitting element) may be obtained, instead of the LED array chip.

(4) According to the embodiment, the cylinder member is formed by removing an unnecessary area of all of the layers 112, 114, 116, 118, 120, 122 and 124 making up the semiconductor multilayer film (see step H in Fig.11). However, it may not be all of these layers which are removed. (However, the division grooves 8, 10 and 11 need to be formed by removing corresponding areas of all of these layers.) Alternatively, the cylinder member 6 can be formed by removing an unnecessary area of the layers from an outmost layer (the n^+-GaN layer 124) to a conductive layer between the light emitting layer 18 and the SiC substrate 104 (the n-GaN clad layer 116). As long as the unnecessary area of these layers 124, 122, 120, 118 and 116 is removed, a side surface of the light emitting layer is exposed on a side surface of the cylinder member. Furthermore, the phosphor film can be formed, at a large thickness, not only on the upper main

surface of the outmost layer but also on the side surface of the cylinder member. As a consequence, unevenness of color can be reduced.

(5) According to the embodiment, the SiC substrate 104 is used as a base substrate for forming, by crystal growth, the semiconductor multilayer film made up of the n-AlGaN buffer layer to the p-GaN contact layer. The reason for this is explained in the following. The SiC substrate has equal or higher heat conductivity compared with copper and aluminum. This feature enables heat generated within the light emitting layer to be effectively conducted to the ceramics substrate, which is a printed-wiring board on which the LED array chips are mounted. Accordingly, the SiC substrate can be replaced with any of an AlN substrate, a GaN substrate, a BN substrate and an Si substrate which similarly have high heat conductivity.

[0056]

Alternatively, the SiC substrate can be replaced with a common sapphire substrate to realize the present invention, even though the sapphire substrate has slightly lower heat conductivity.

(6) According to the embodiment, the LED array chip is a square approximately 2 mm on a side. However, the embodiment is not limited to such.

(7) According to the embodiment, depressions are formed by providing the n^+-GaN regrowth layer, in order to improve light extraction efficiency. However, the embodiment is not limited to such. The depressions may be formed in a different manner. For example, a pattern mask is formed on the p-GaN contact layer and etching is then conducted. Alternatively, a dielectric layer made of, for

example, Ta_2O_5 is formed on the p-GaN contact layer. After this, a pattern mask is formed on the dielectric layer and etching is then conducted.

[INDUSTRIAL APPLICABILITY]

[0057]

As described above, a semiconductor light emitting device of the present invention is applicable in, for example, the field of lighting that requires a spot shape which is more like a circle than a substantially circular shape or rectangular shape.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[0058]

Fig.1 is a perspective view illustrating an LED array chip.

Fig.2 is a plan view illustrating the LED array chip.

Fig.3A illustrates a cross-section of the LED array chip along a line A-A shown in Fig.1B, and Fig. 3B illustrates a cross-section of the LED array chip along a line B-B shown in Fig.1B.

Fig.4A illustrates how LEDs are connected in the LED array chip, and Fig.4B is a bottom plan view illustrating the LED array chip.

Fig.5 is used to describe a manufacturing method of the LED array chip.

Fig.6 is used to describe the manufacturing method of the LED array chip.

Fig.7 is used to describe the manufacturing method of the LED array chip.

Fig.8 is used to describe the manufacturing method of the LED array chip.

Fig.9 is used to describe the manufacturing method of the LED array chip.

Fig.10 illustrates part of the manufacturing method of the LED array chip.

Fig.11 illustrates part of the manufacturing method of the LED array chip.

Fig.12 illustrates part of the manufacturing method of the LED array chip.

Fig.13 illustrates part of the manufacturing method of the LED array chip.

Fig.14 is a perspective view illustrating an LED module.

Fig.15A is a plan view illustrating the LED module, Fig.15B illustrates a cross-section of the LED module along a line E-E shown in Fig.15A, and Fig.15C is an enlarged view illustrating a portion F shown in Fig.15B.

Fig.16A illustrates the LED module after removing a lens, and Fig.16B illustrates a pad pattern formed on a ceramics substrate constituting the LED module.

Fig.17A is a perspective view illustrating a lighting apparatus, and Fig.17B is a bottom plan view illustrating the lighting apparatus.

Fig.18 is a perspective exploded view illustrating the lighting apparatus.

Fig.19 shows an emission spectrum of the lighting apparatus.

[DESCRIPTION OF CHARACTERS]

[0059]

4 SiC substrate

6 cylinder member

8, 10, 11 division groove

14 DBR layer composed of 30 periods of n-AlGaN/GaN

18 InGaN/GaN MQW light emitting layer

50 phosphor film

[DOCUMENT] Abstract

[SUMMARY]

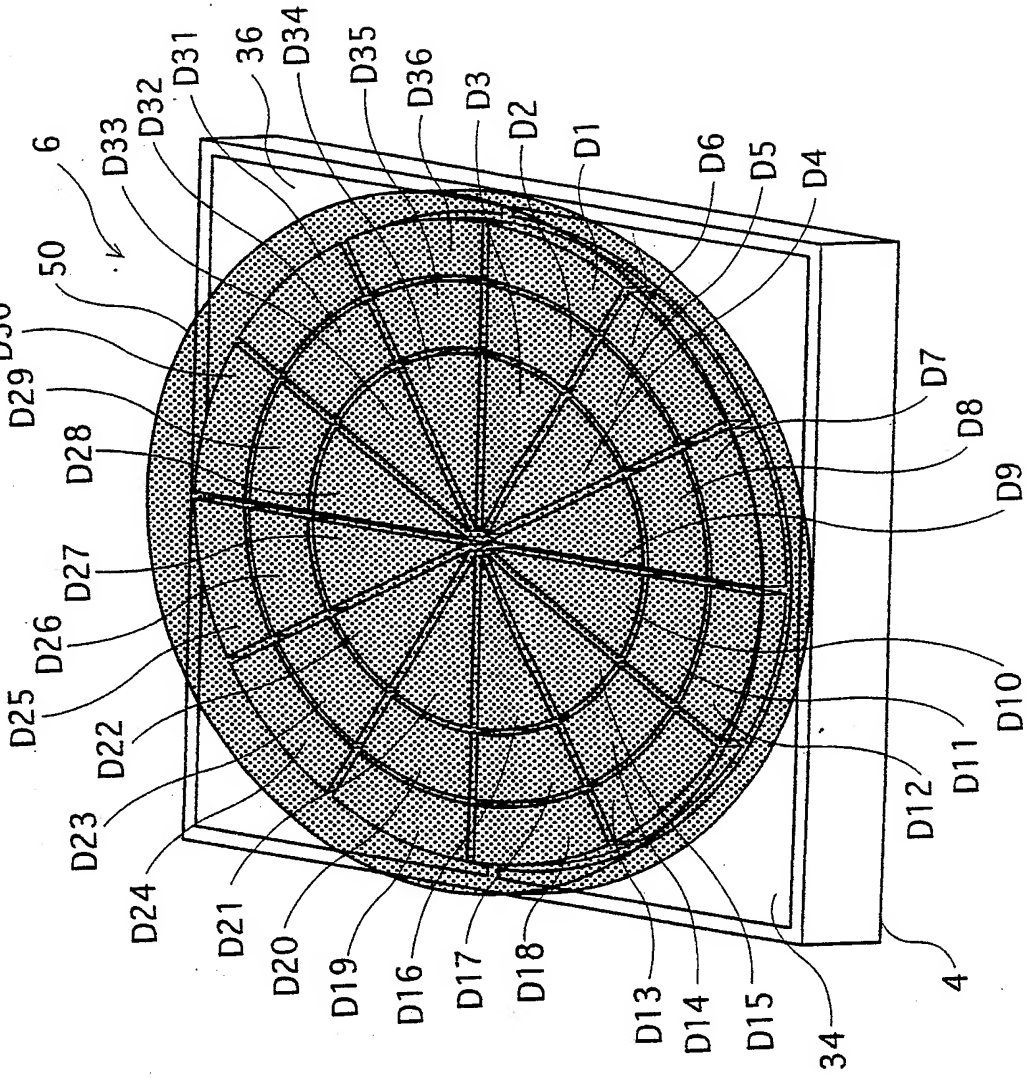
[PROBLEM] Providing a semiconductor light emitting device whose beam has a substantially circular spot shape.

[MEANS TO SOLVE THE PROBLEM] An LED array chip 2 (semiconductor light emitting device) has an LED array composed of an SiC substrate 4 and 36 LEDs (D1 to D36) that have been formed by crystal growth on the SiC substrate 4. The LED array is formed like a circular cylinder as a whole. Such circular cylinder member is covered by a phosphor film 50 such that the thickness is substantially even.

[SELECTED FIGURE] Fig.1

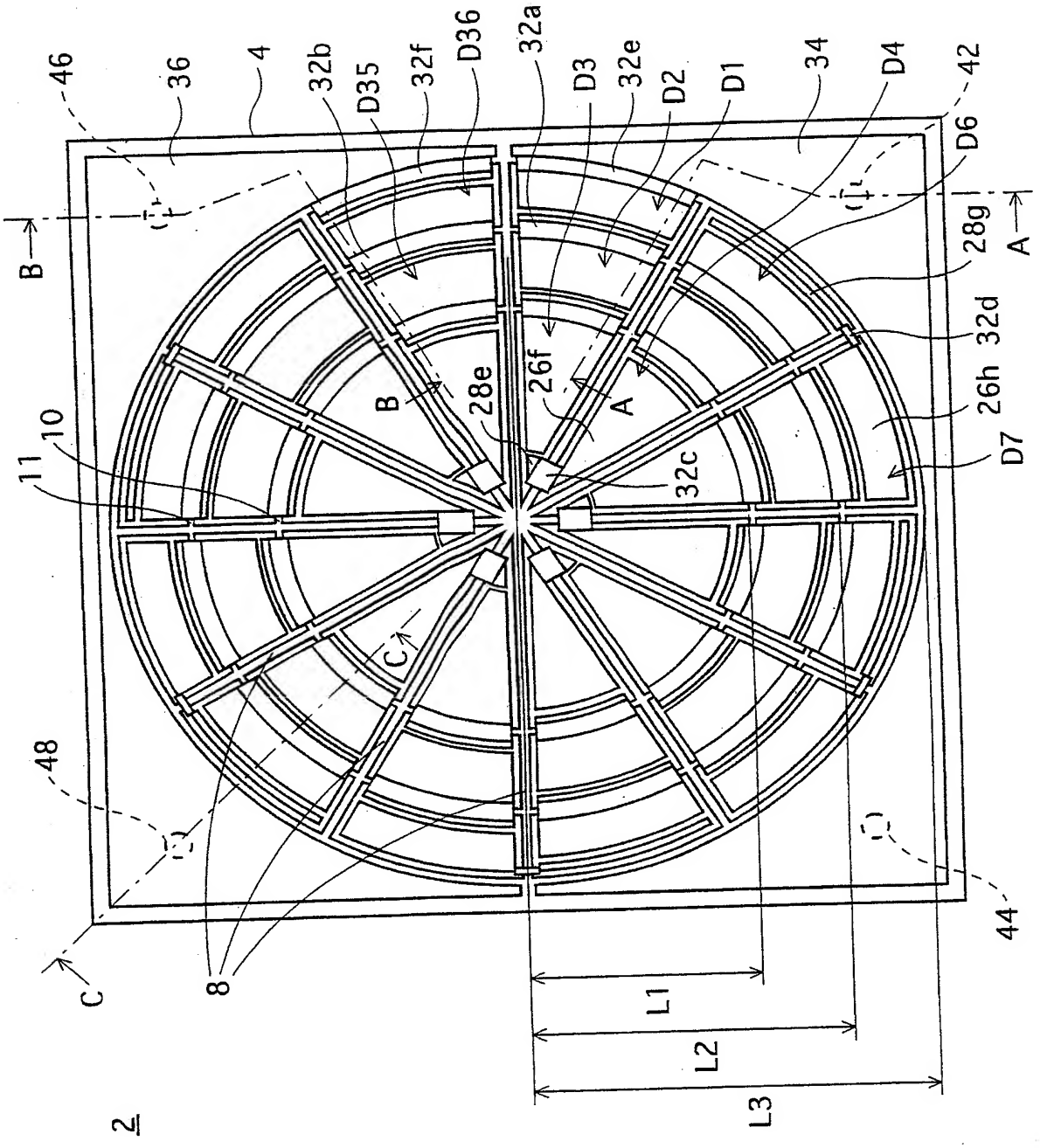
[DOCUMENT] Drawings

FIG. 1



2

FIG. 2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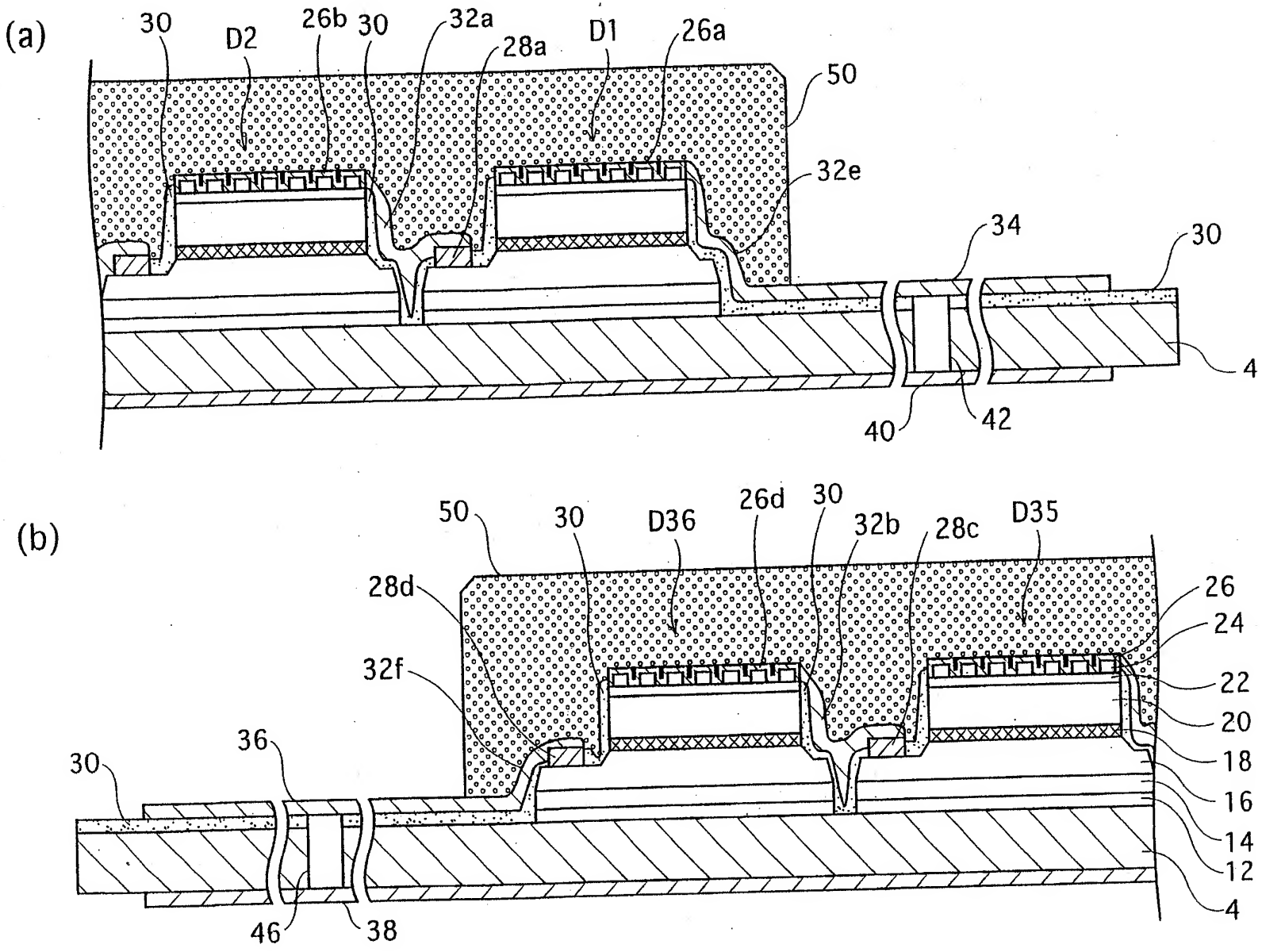
46
36
4
32b
D35
32f
D36
32a
D3
32e
D2
D1
34
D4
42
D6
28g
A
B
32d
26f
28e
B
A
26h
D7
11
10
32c
C
48
C
8
44
L1
L2
L3

FIG. 3


(a)
30
D2
26b
30
32a
28a
D1
26a
50
32e
34
30
4
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42
(b)
50
30
D36
26d
30
32b
28c
D35
28d
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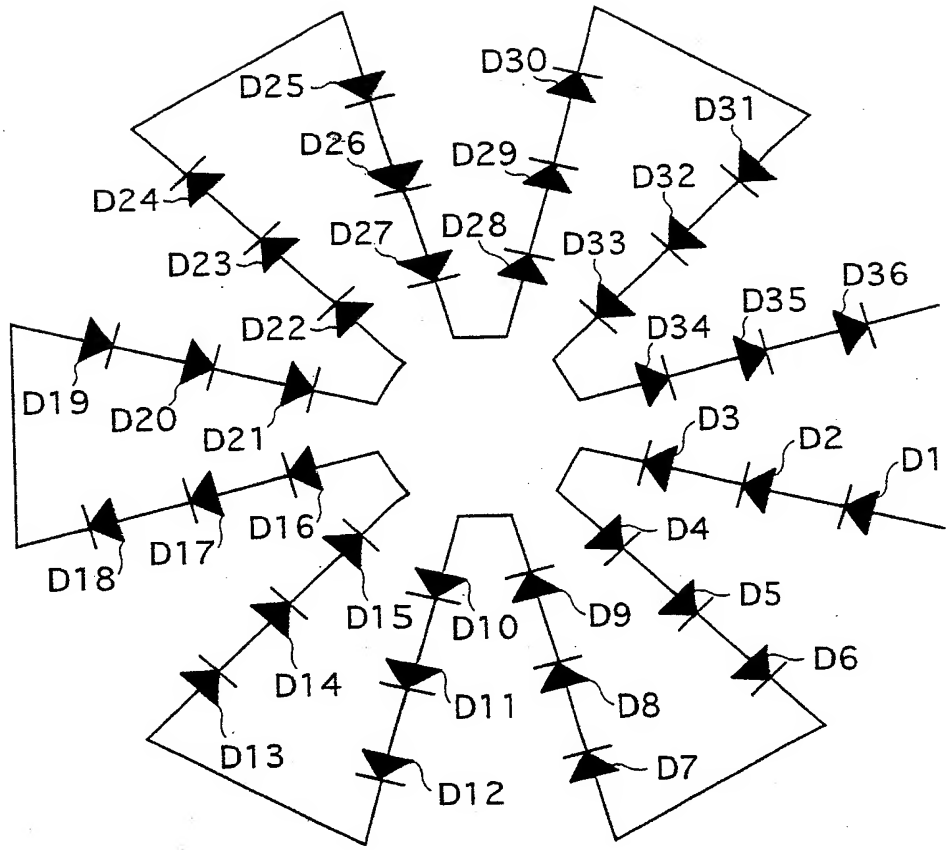
4
46
38

FIG. 4

(a)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D16
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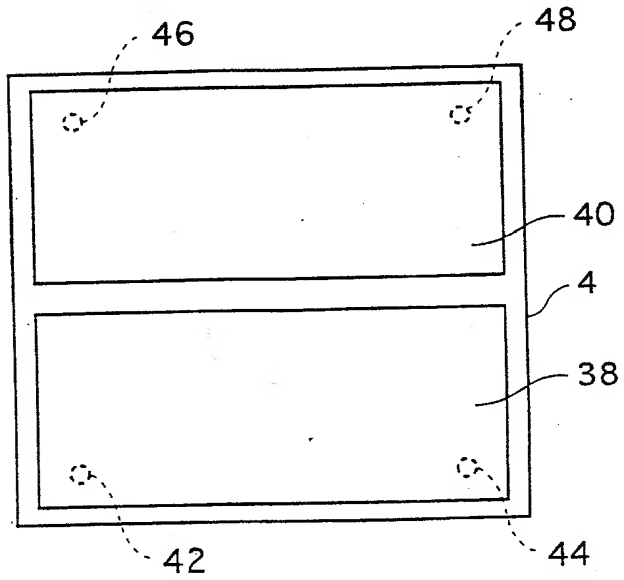
D12
D7

(b)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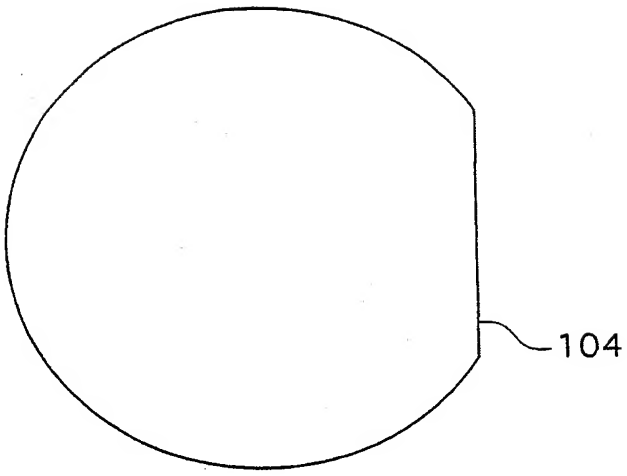
38
42
44

FIG. 5

(a)



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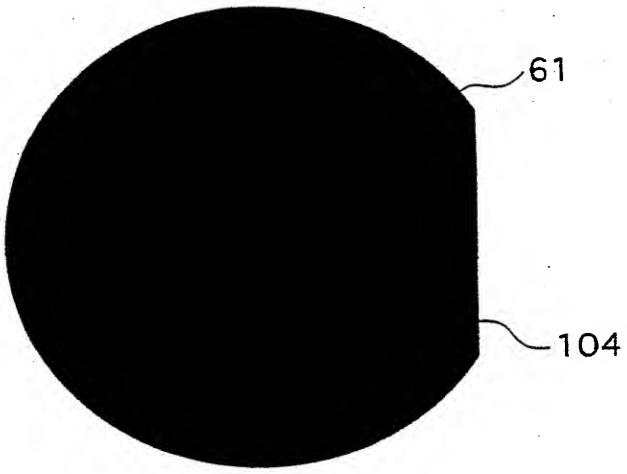


FIG. 6

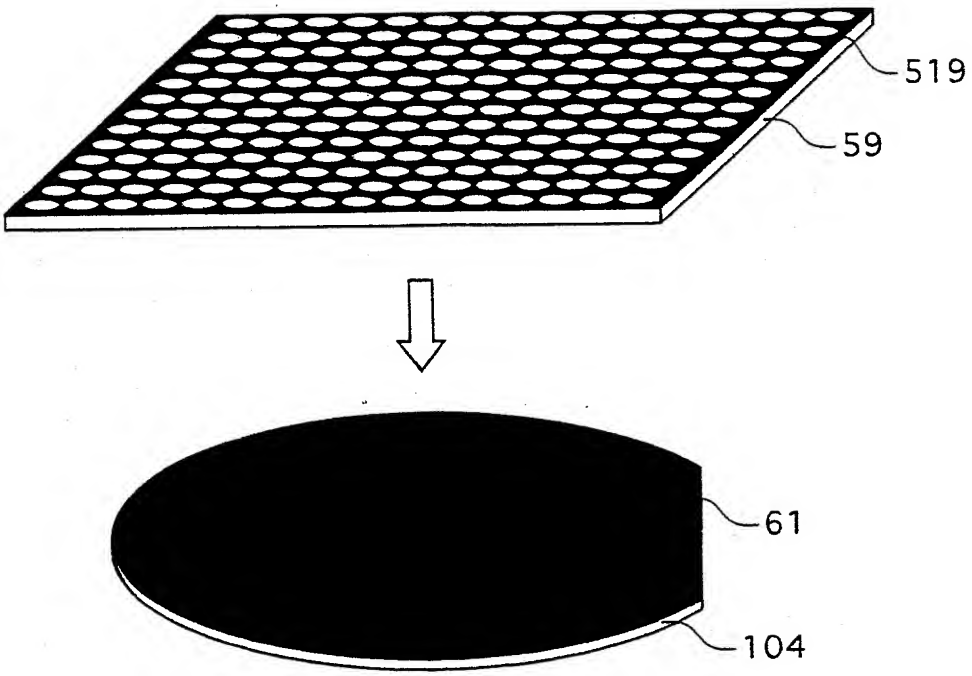
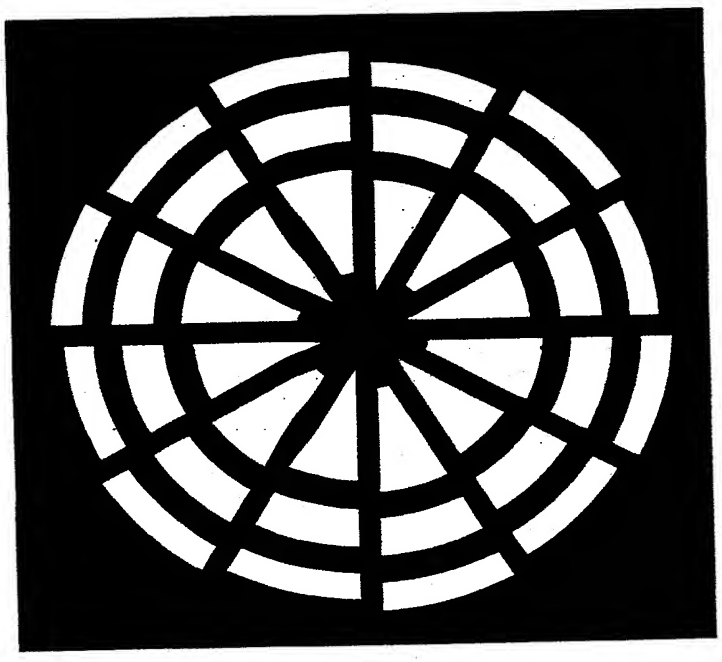


FIG. 7

(a)



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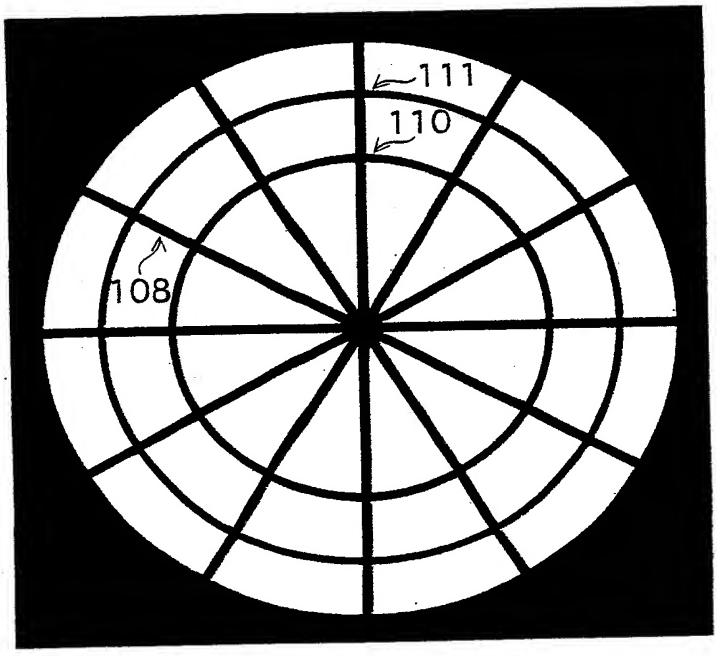
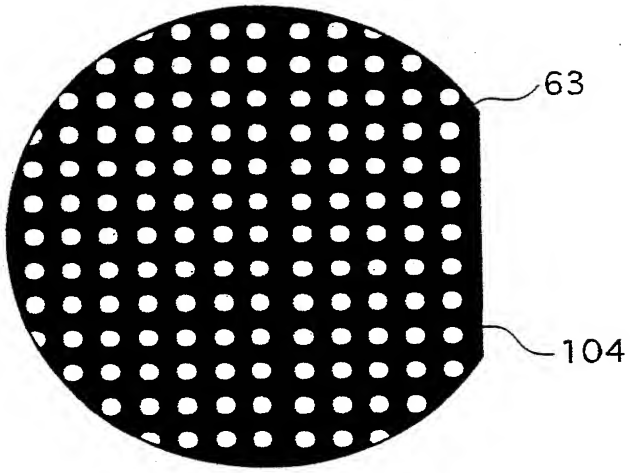


FIG. 8

(a)



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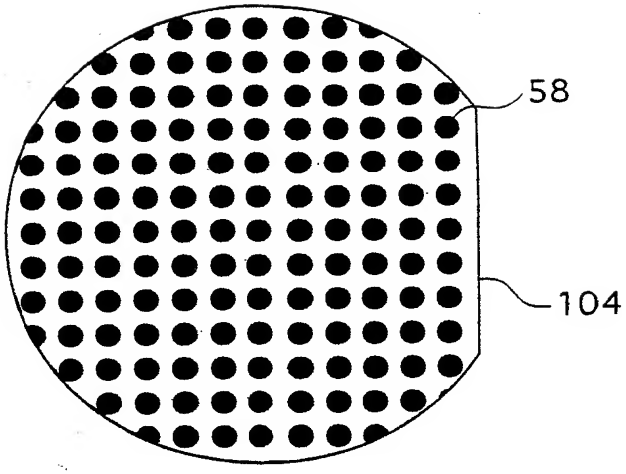
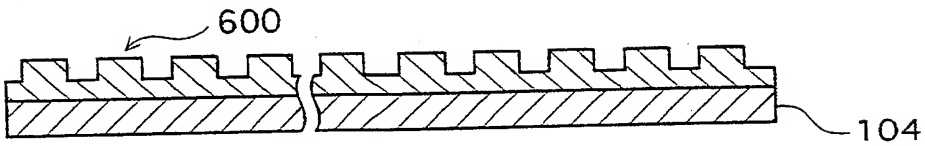


FIG. 9

(a)



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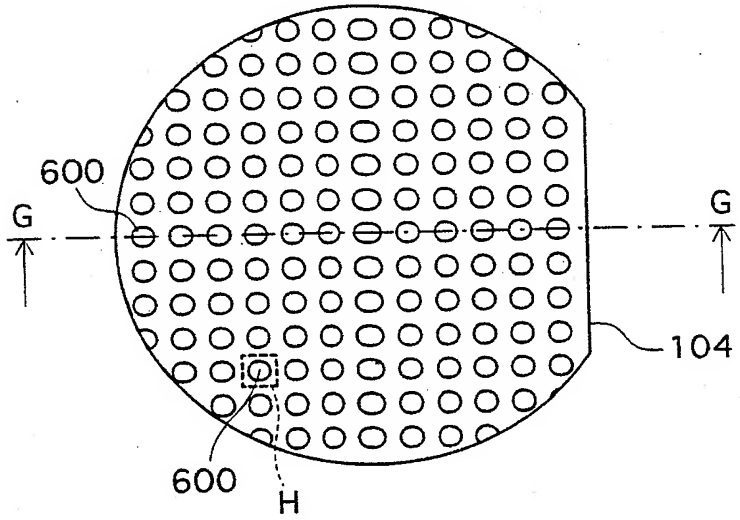


(c)

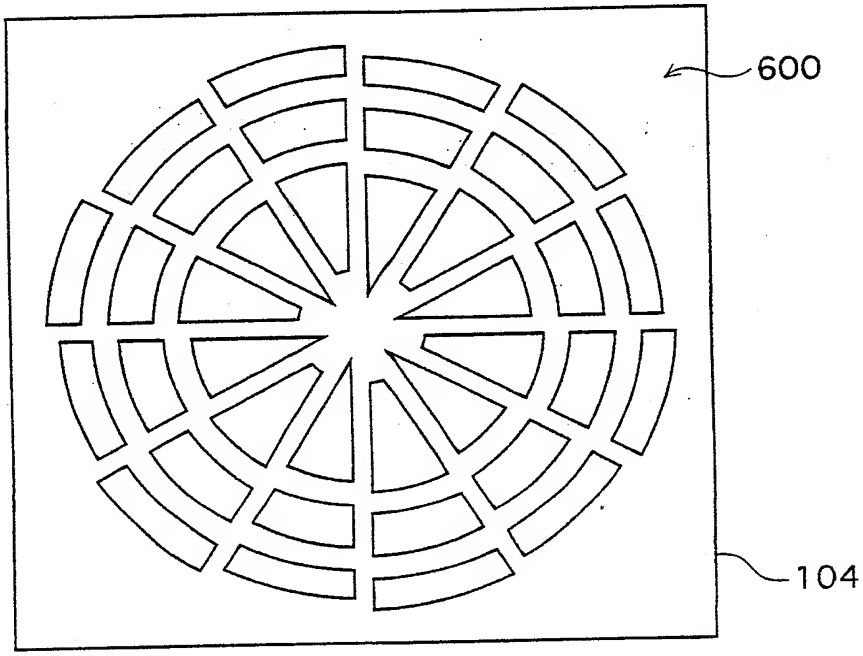
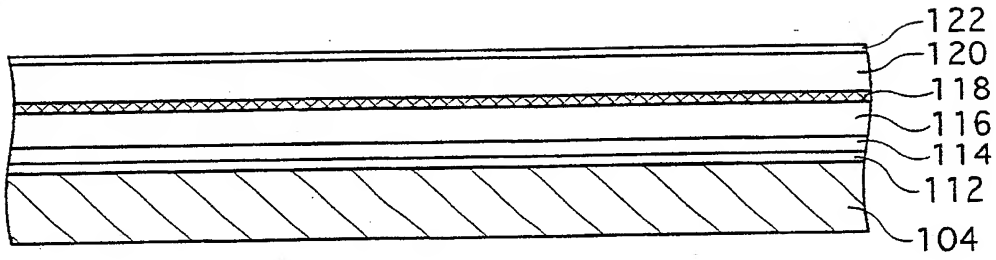
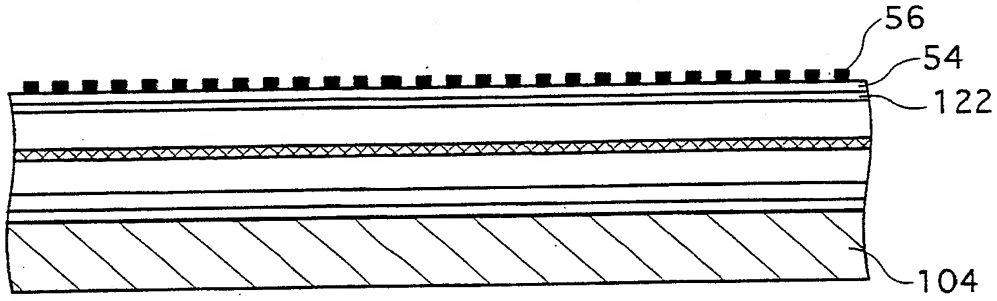


FIG. 10

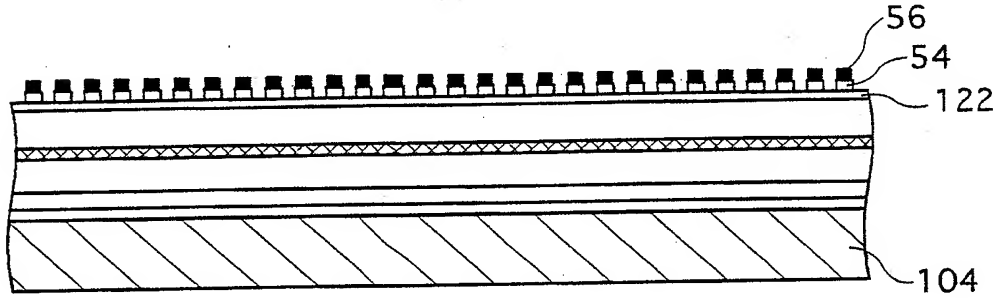
(a)



(b)



(c)



(d)

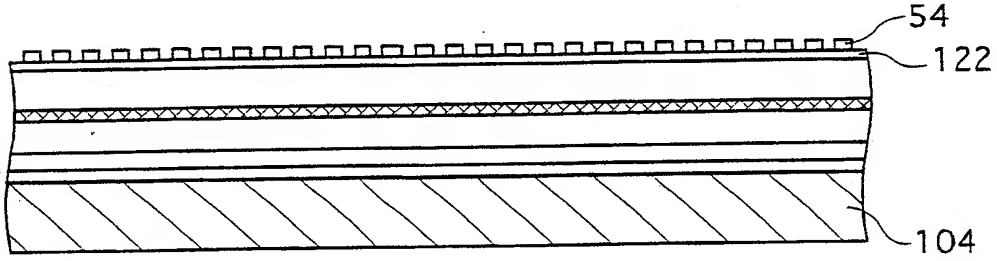
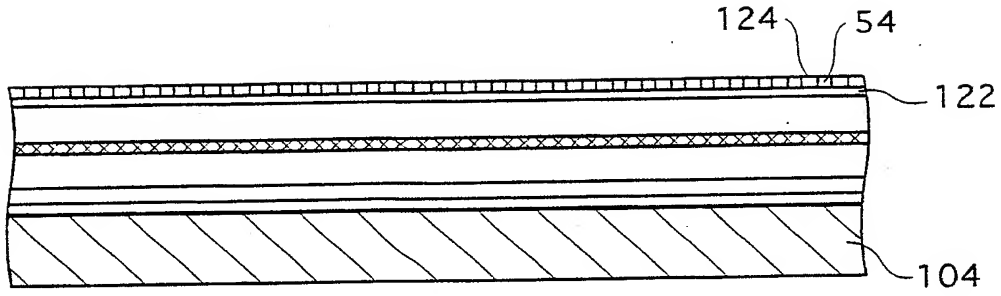
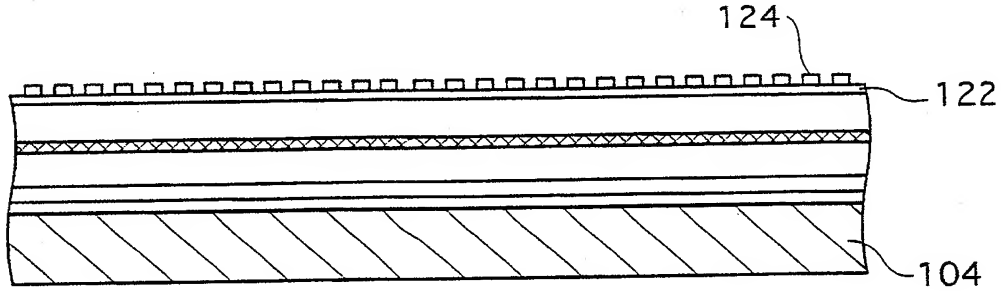


FIG. 11

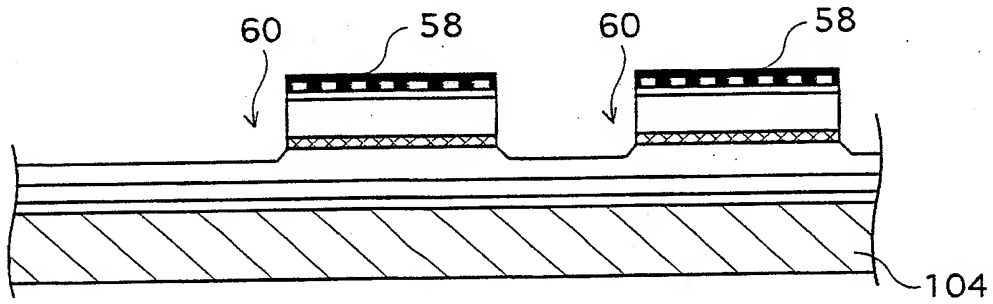
(e)



(f)



(g)



(h)

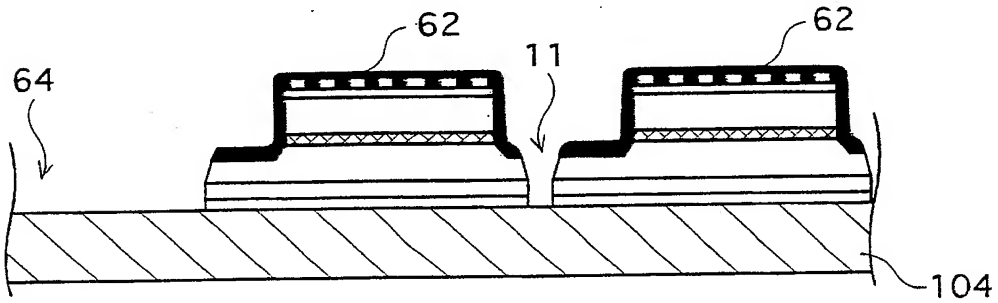
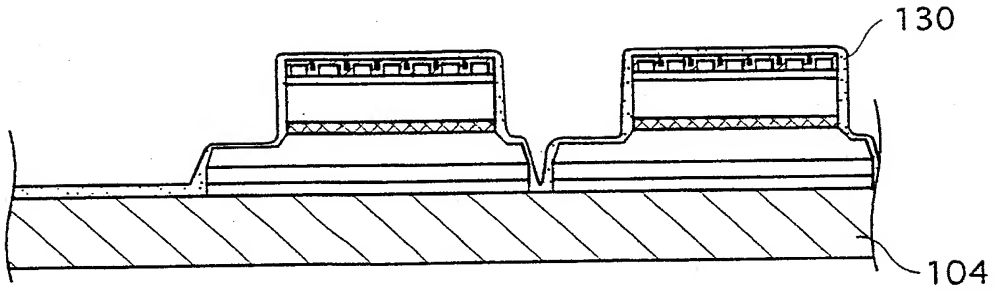
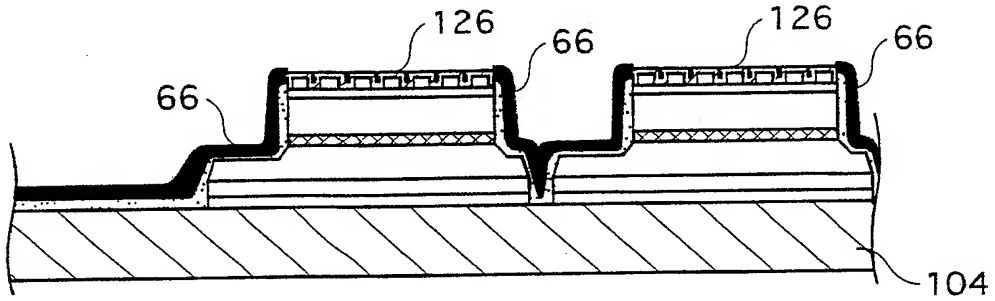


FIG. 12

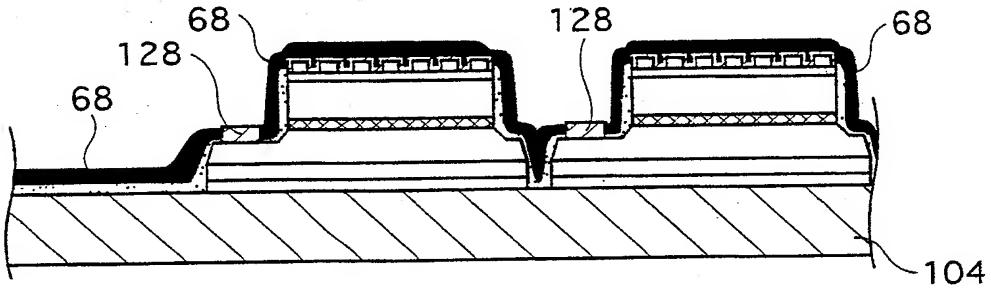
(i)



(j)



(k)



(l)

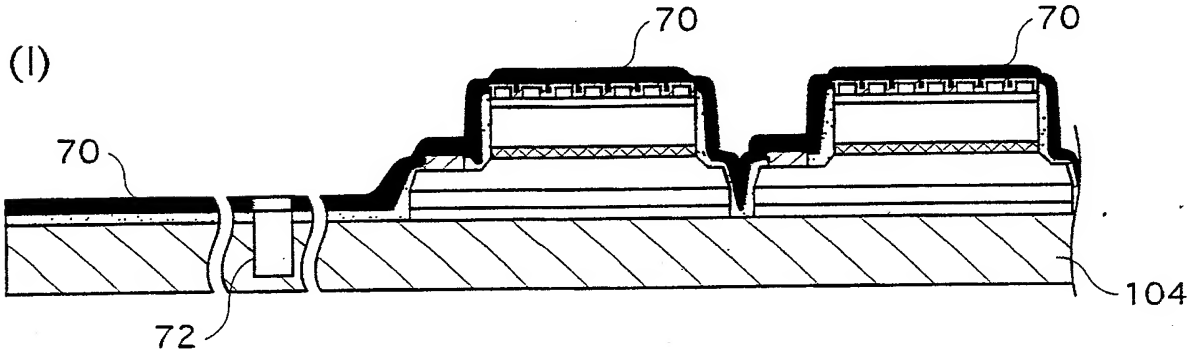


FIG. 13

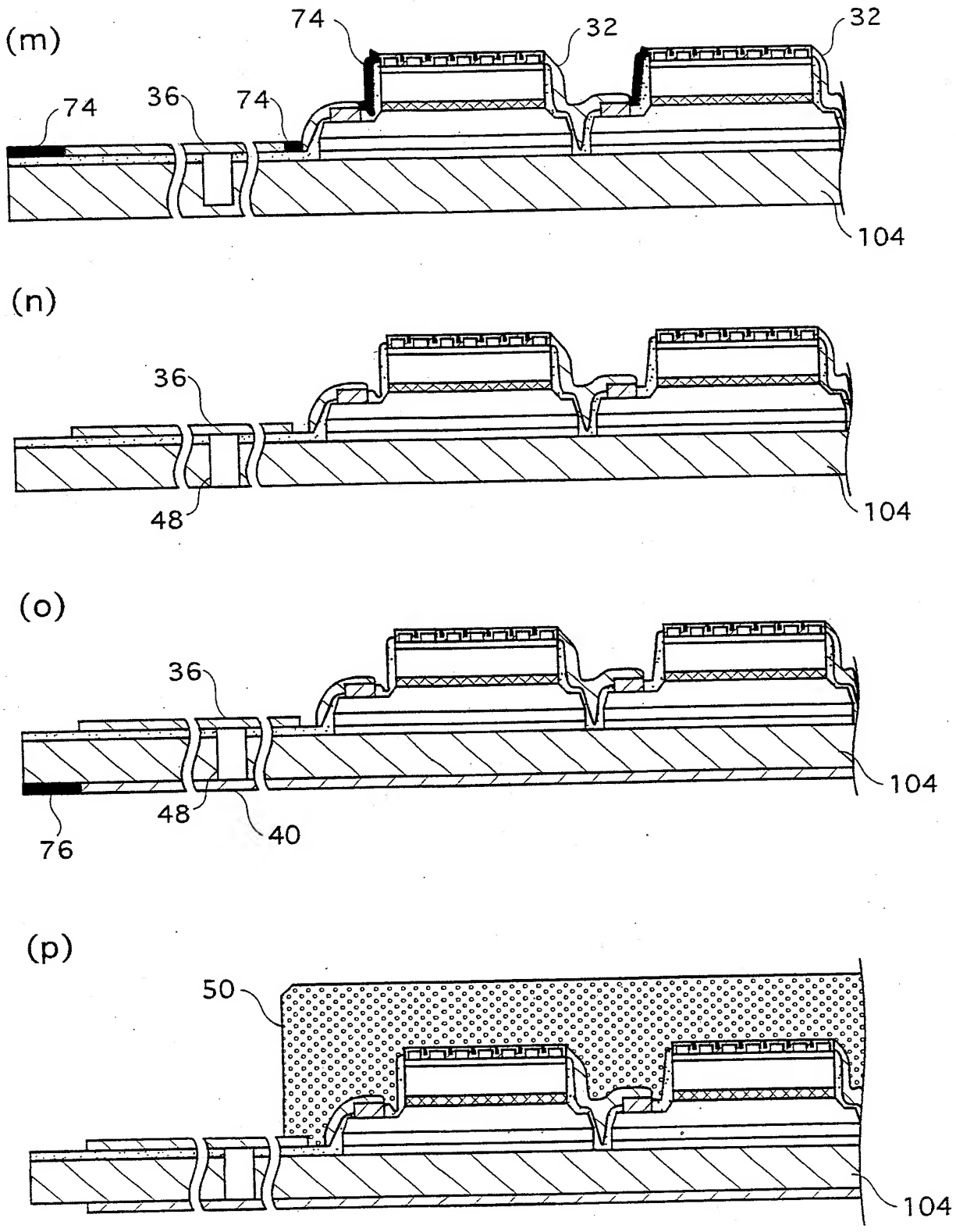


FIG. 14

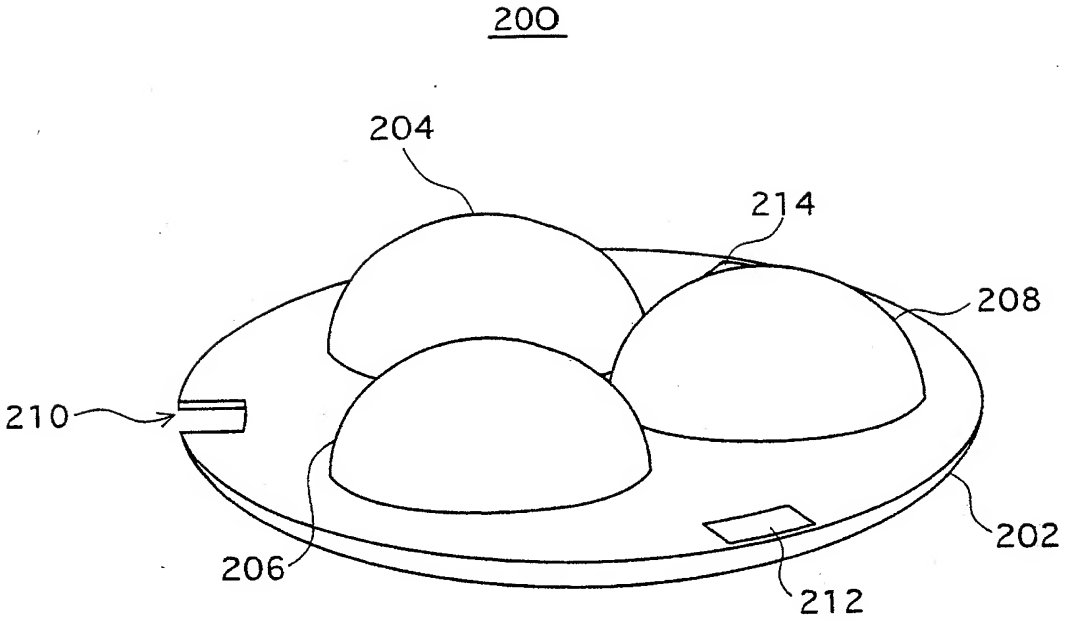


FIG. 15

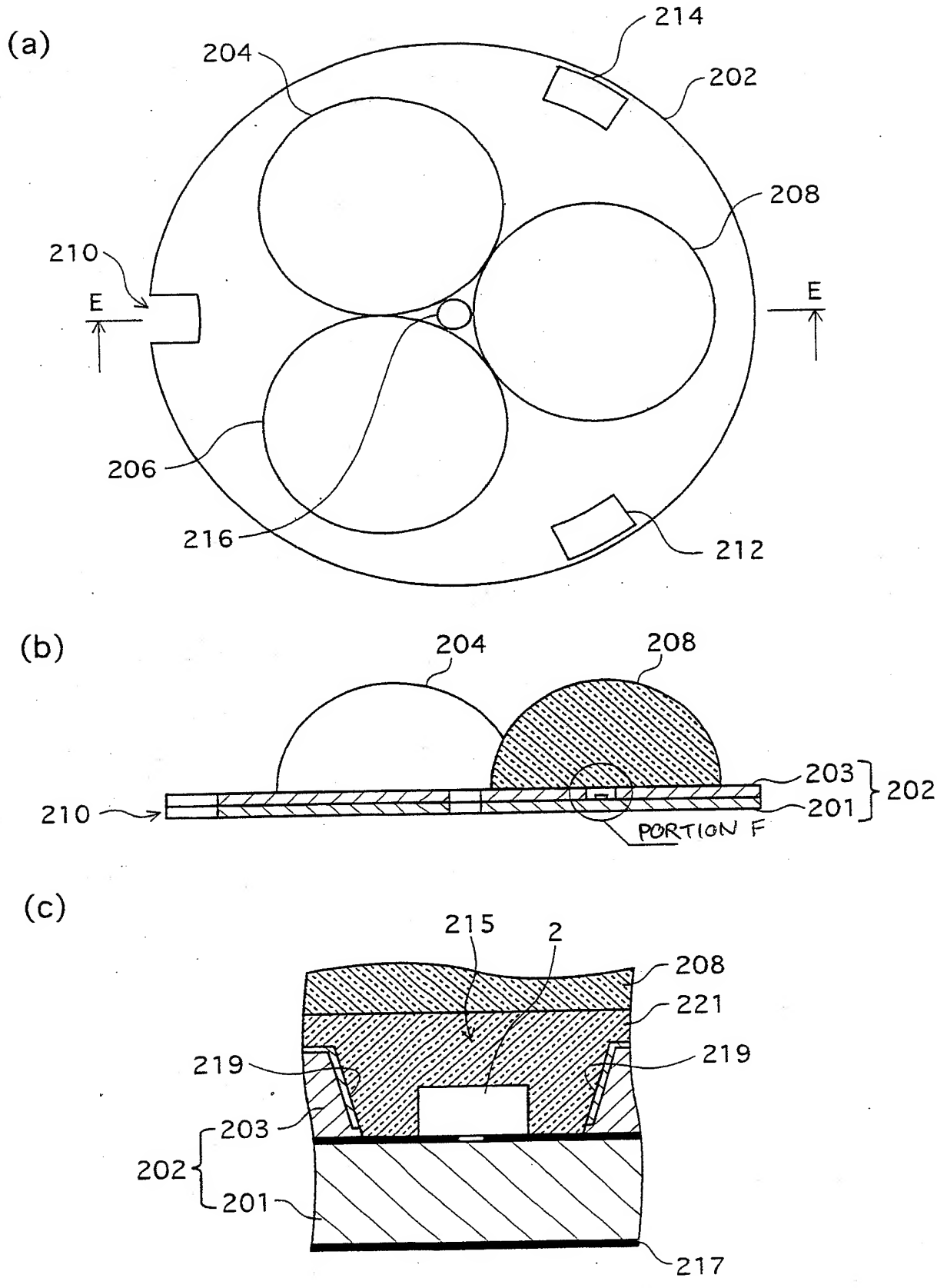
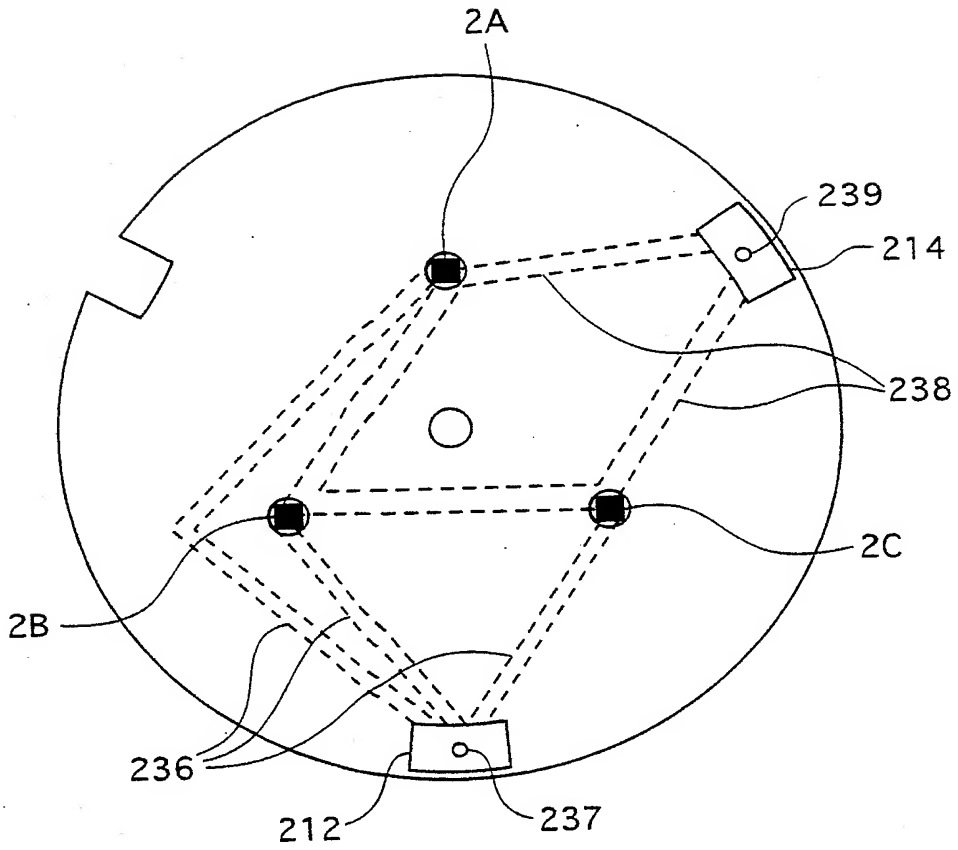

(a)
214
204
202
208
210
E
E
206
216
212
(b)
204
208
203
202
210
201
PORTION F
(c)
215
2
208
221
219
219
203
202
201
217

FIG. 16

(a)



(b)

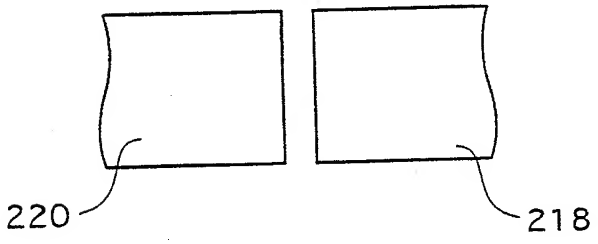
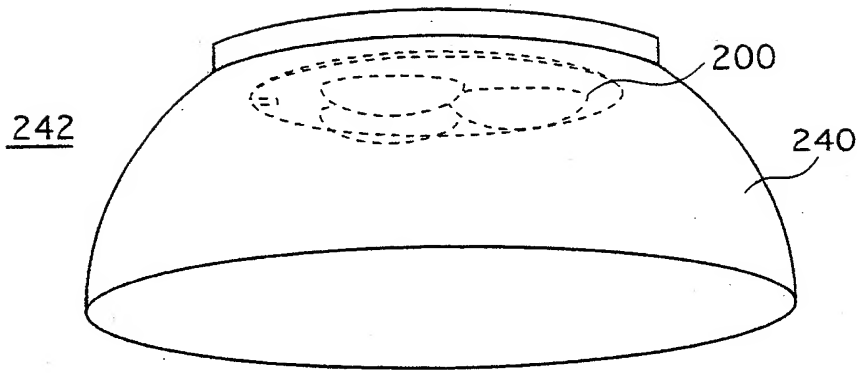


FIG. 17

(a)



(b)

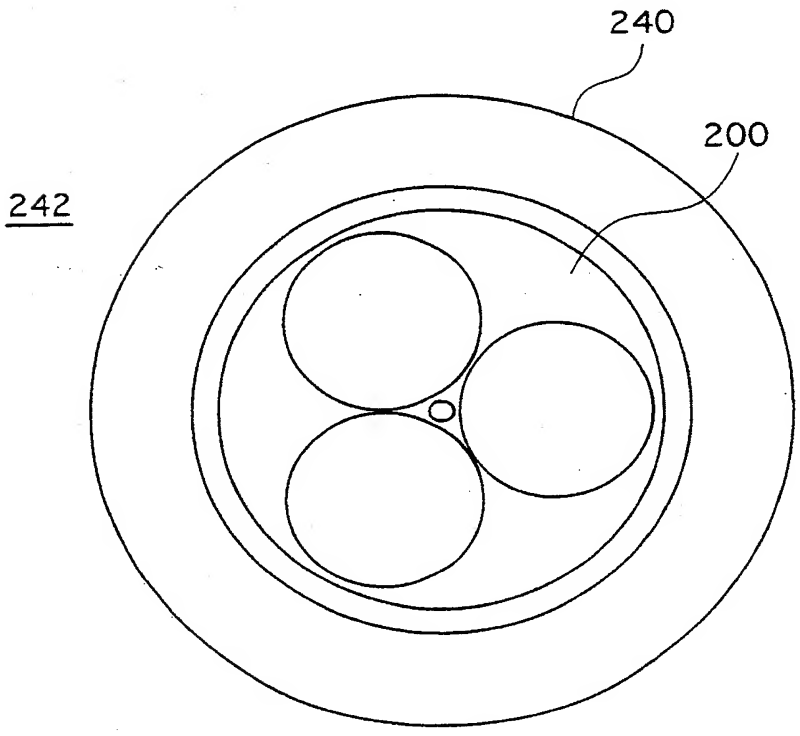


FIG. 18

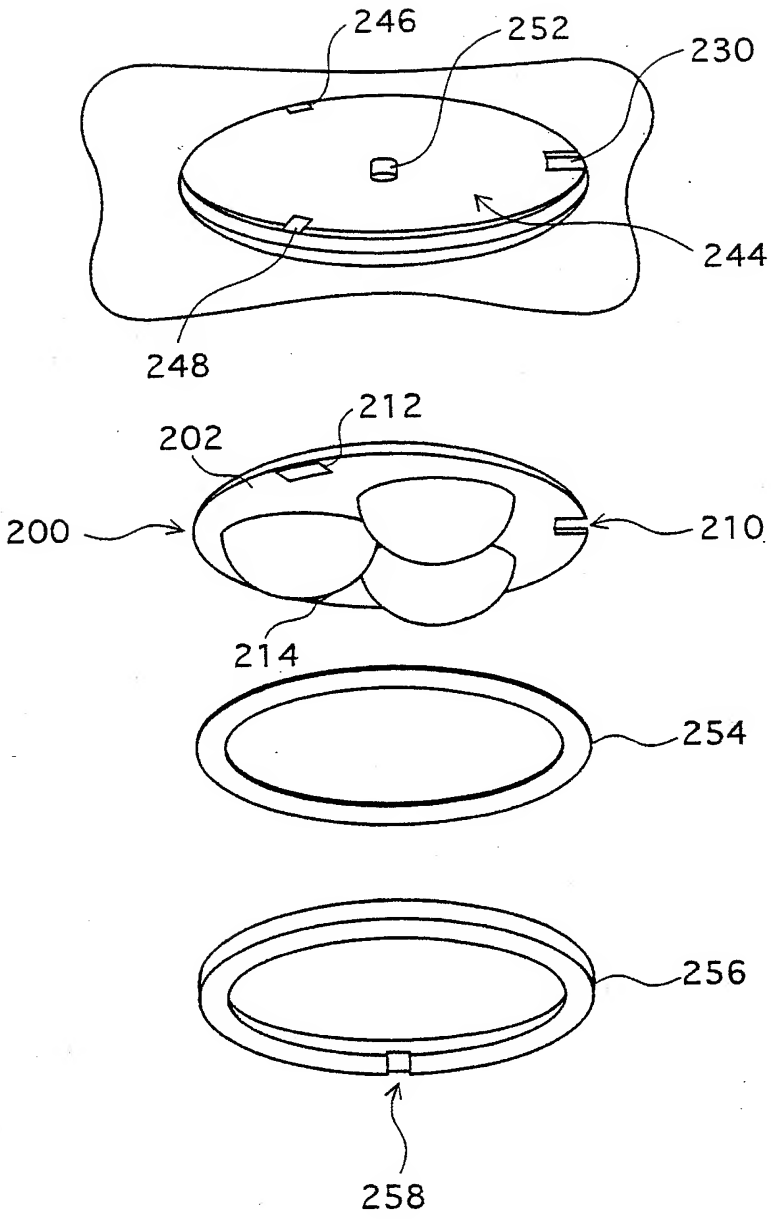
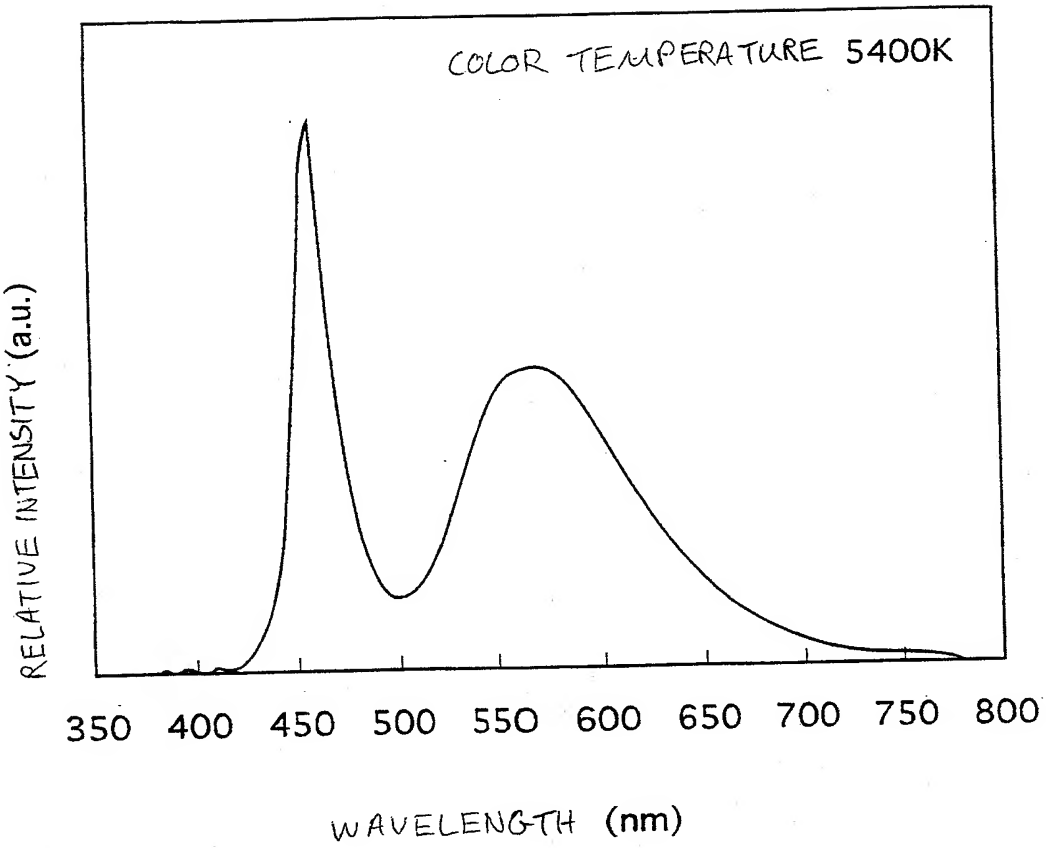


FIG. 19


COLOR TEMPERATURE 5400K
RELATIVE INTENSITY (a.u.)
350
400
450
500
550
600
650
700
750
800
WAVELENGTH (nm)